

FEATURES**44 V supply maximum ratings** **V_{SS} to V_{DD} analog signal range****Low on resistance (12 Ω typ)****Low ΔR_{ON} (3 Ω max)****Low R_{ON} match (2.5 Ω max)****Low power dissipation****Fast switching times** $t_{ON} < 175 \text{ ns}$ $t_{OFF} < 145 \text{ ns}$ **Low leakage currents (5 nA max)****Low charge injection (10 pC)****Break-before-make switching action****APPLICATIONS****Audio and video switching****Battery-powered systems****Test equipment****Communications systems****GENERAL DESCRIPTION**

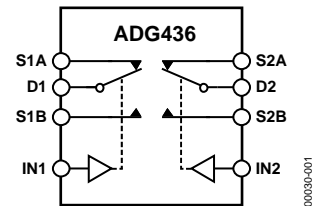
The ADG436 is a monolithic CMOS device comprising two independently selectable SPDT switches. It is designed on an LC²MOS process, which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on and has an input signal range which extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Rev. B

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FUNCTIONAL BLOCK DIAGRAM*Figure 1.***PRODUCT HIGHLIGHTS**

1. Extended signal range.
The ADG436 is fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. Low power dissipation.
3. Low R_{ON} .
4. Single-supply operation.
For applications where the analog signal is unipolar, the ADG436 can be operated from a single rail power supply.

ADG436* Product Page Quick Links

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TABLE OF CONTENTS

| | | | |
|--|---|---|----|
| Specifications..... | 3 | Typical Performance Characteristics | 8 |
| Dual Supply | 3 | Test Circuits..... | 10 |
| Single Supply | 4 | Applications Information | 11 |
| Absolute Maximum Ratings..... | 5 | ADG436 Supply Voltages | 11 |
| ESD Caution..... | 5 | Power-Supply Sequencing..... | 11 |
| Pin Configuration and Function Descriptions..... | 6 | Outline Dimensions | 12 |
| Terminology | 7 | Ordering Guide | 12 |

REVISION HISTORY

3/05—Rev. A to Rev. B

| | |
|---------------------------------------|-----------|
| Updated Format..... | Universal |
| Changes to Specifications Tables..... | 3 |
| Changes to Figure 11..... | 8 |
| Updated Outline Dimensions | 12 |
| Changes to Ordering Guide | 12 |

11/98—Rev. 0 to Rev. A

1/96—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY¹

$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | Unit | Test Conditions/ Comments |
|--|-------------|----------------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{SS} to V_{DD} | V | |
| R_{ON} | 12 | | Ω typ | $V_D = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | | | Ω max | |
| ΔR_{ON} | 1 | 25 | Ω typ | $V_D = -5\text{ V}$, 5 V , $I_S = -10\text{ mA}$ |
| | | | Ω max | |
| $R_{ONMatch}$ | 1 | 3 | Ω typ | $V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | | | Ω max | |
| | | 2.5 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.005 | | nA typ | $V_{DD} = 16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 0.25 | ± 5 | nA max | $V_D = \pm 15.5\text{ V}$, $V_S = \pm 15.5\text{ V}$ |
| Channel ON Leakage I_D , I_S (ON) | ± 0.05 | | nA typ | Figure 13 |
| | ± 0.4 | ± 5 | nA max | $V_S = V_D = \pm 15.5\text{ V}$ |
| | | | | Figure 14 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | | ± 0.005 | μA typ | $V_{IN} = 0\text{ V}$ or V_{DD} |
| | | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 70 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | 125 | ns max | $V_S = \pm 10\text{ V}$; Figure 15 |
| t_{OFF} | 60 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | 120 | ns max | $V_S = \pm 10\text{ V}$; Figure 15 |
| Break-Before-Make Delay, t_{OPEN} | 10 | | ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | | | $V_S = +5\text{ V}$; Figure 16 |
| Charge Injection | 10 | | pC typ | $V_D = 0\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$; |
| | | | | Figure 17 |
| OFF Isolation | 72 | | dB typ | $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; |
| | | | | $V_S = 2.3\text{ V rms}$, Figure 18 |
| Channel-to-Channel Crosstalk | 90 | | dB typ | $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; |
| | | | | $V_S = 2.3\text{ V rms}$, Figure 19 |
| C_S (OFF) | 13 | | pF typ | |
| C_D , C_S (ON) | 49 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.05 | | mA typ | Digital inputs = 0 V or 5 V |
| | | 0.35 | mA max | |
| I_{SS} | 0.01 | | μA typ | |
| | 1 | 5 | μA max | |
| V_{DD}/V_{SS} | | $\pm 3/\pm 20$ | V min/V max | $ V_{DD} = V_{SS} $ |

¹ Temperature range is as follows: B version, -40°C to $+85^\circ\text{C}$.

² Guaranteed by design; not subject to production test.

ADG436

SINGLE SUPPLY¹

$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | −40°C to +85°C | Unit | Test Conditions/ Comments |
|--|-------------|----------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to V_{DD} | V | |
| R_{ON} | 20 | 40 | Ω typ | $V_D = 1\text{ V}$, 10 V, $I_S = -1\text{ mA}$ |
| $R_{ONMatch}$ | | 2.5 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source OFF Leakage I_S (OFF) | ± 0.005 | | nA typ | $V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$ |
| | ± 0.25 | ± 5 | nA max | Figure 13 |
| Channel ON Leakage I_D , I_S (ON) | ± 0.05 | | nA typ | $V_S = V_D = 12.2\text{ V}/1\text{ V}$ |
| | ± 4 | ± 5 | nA max | Figure 14 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | | ± 0.005 | μA typ | $V_{IN} = 0\text{ V}$ or V_{DD} |
| | | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 100 | 200 | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | | ns max | $V_S = 8\text{ V}$; Figure 15 |
| t_{OFF} | 90 | 180 | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | | ns max | $V_S = 8\text{ V}$; Figure 15 |
| Break-Before-Make Delay, t_{OPEN} | 10 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; |
| | | | | $V_S = 5\text{ V}$; Figure 16 |
| Charge Injection | 10 | | pC typ | $V_D = 6\text{ V}$, $R_D = 0\ \Omega$, $C_L = 10\text{ nF}$; Figure 17 |
| OFF Isolation | 72 | | dB typ | $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; |
| | | | | $V_S = 1.15\text{ V rms}$; Figure 18 |
| Channel-to-Channel Crosstalk | 90 | | dB typ | $R_L = 75\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; |
| | | | | $V_S = 1.15\text{ V rms}$, Figure 19 |
| C_S (OFF) | 22 | | pF typ | |
| C_D , C_S (ON) | 46 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.05 | 0.35 | mA typ | $V_{DD} = 13.5\text{ V}$ |
| | | | mA max | Digital inputs = 0 V or 5 V |
| V_{DD} | | +3/+30 | V min/V max | |

¹ Temperature range is as follows: B version, -40°C to $+85^\circ\text{C}$.

² Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|---|
| V_{DD} to V_{SS} | +44 V |
| V_{DD} to GND | -0.3 V to +30 V |
| V_{SS} to GND | +0.3 V to -30 V |
| Analog, Digital Inputs ¹ | $V_{SS} - 2\text{ V}$ to $V_{DD} + 2\text{ V}$ or 20 mA, whichever occurs first |
| Continuous Current, S or D | 20 mA |
| Peak Current, S or D (pulsed at 1 ms, 10% Duty Cycle max) | 40 mA |
| Operating Temperature Range Industrial (B Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +125°C |
| Junction Temperature | 150°C |
| θ_{JA} , Thermal Impedance | |
| PDIP Package | 117°C/W |
| SOIC Package | 77°C/W |
| Lead Temperature, Soldering (10 sec) | 260°C |
| Lead Temperature, Soldering Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 4. Truth Table

| Logic | Switch A | Switch B |
|-------|----------|----------|
| 0 | Off | On |
| 1 | On | Off |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADG436

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

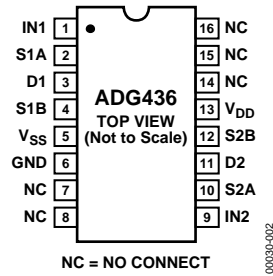


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Descriptions |
|------------------|--------------------|--|
| 1, 9 | IN1, IN2 | Logic Control Input. |
| 2, 4, 10, 12 | S1A, S1B, S2A, S2B | Source Terminal. Can be an input or output. |
| 3, 11 | | Drain Terminal. C be an input or output. |
| 5 | V _{SS} | Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground. |
| 6 | GND | Ground (0 V) Reference. |
| 7, 8, 14, 15, 16 | NC | No Connect. |
| 13 | V _{DD} | Most Positive Power Supply Potential. |

TERMINOLOGY

Table 6.

| Mnemonic | Descriptions |
|-------------------------|--|
| R_{ON} | Ohmic resistance between D and S. |
| ΔR_{ON} | R_{ON} variation due to a change in the analog input voltage with a constant load current. |
| $R_{ONMatch}$ | Difference between the R_{ON} of any two channels. |
| I_S (OFF) | Source leakage current with the switch off. |
| I_D, I_S (ON) | Channel leakage current with the switch on. |
| V_D (V_S) | Analog voltage on terminals D, S. |
| C_S (OFF) | OFF switch source capacitance. |
| C_D, C_S (ON) | ON switch capacitance. |
| t_{ON} | Delay between applying the digital control input and the output switching on. |
| t_{OFF} | Delay between applying the digital control input and the output switching off. |
| t_{OPEN} | Break-before-make delay when switches are configured as a multiplexer. |
| V_{INL} | Maximum input voltage for Logic 0. |
| V_{INH} | Minimum input voltage for Logic 1. |
| I_{INL} (I_{INH}) | Input current of the digital input. |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A measure of unwanted signal coupling through an OFF switch. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| I_{DD} | Positive supply current. |
| I_{SS} | Negative supply current. |

TYPICAL PERFORMANCE CHARACTERISTICS

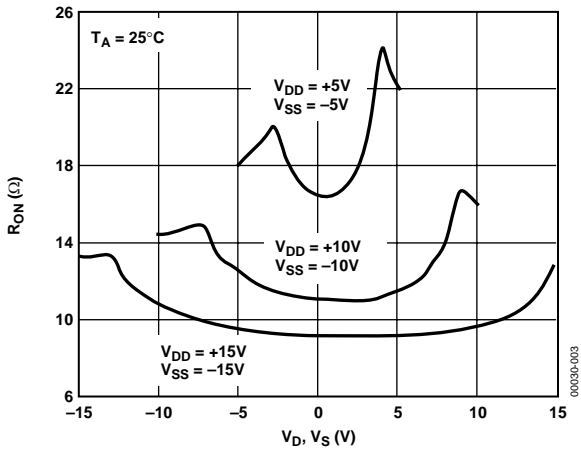


Figure 3. R_{ON} as a Function of $V_D (V_S)$: Dual Supply

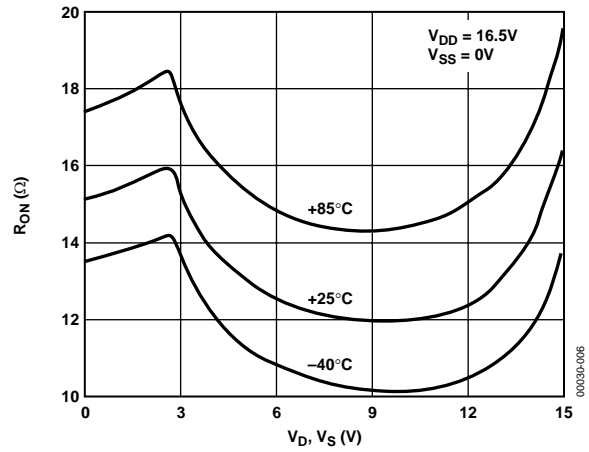


Figure 6. R_{ON} as a Function of $V_D (V_S)$ for Different Temperatures: Single Supply

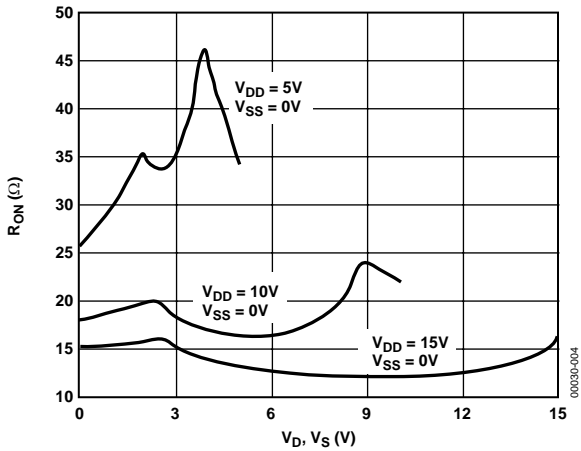


Figure 4. R_{ON} as a Function of $V_D (V_S)$: Single Power Supply

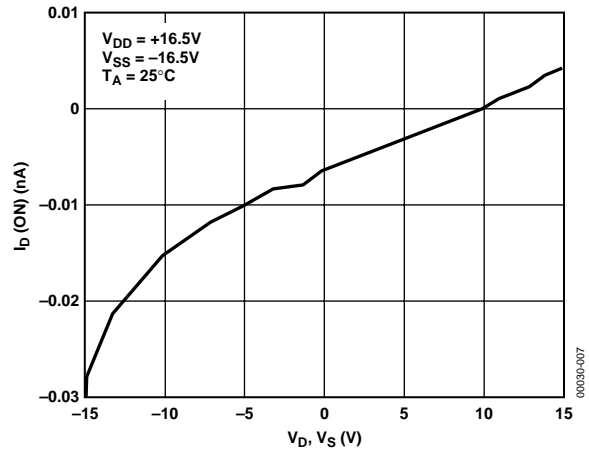


Figure 7. I_D (ON) Leakage Current as a Function of $V_D (V_S)$: Dual Supply

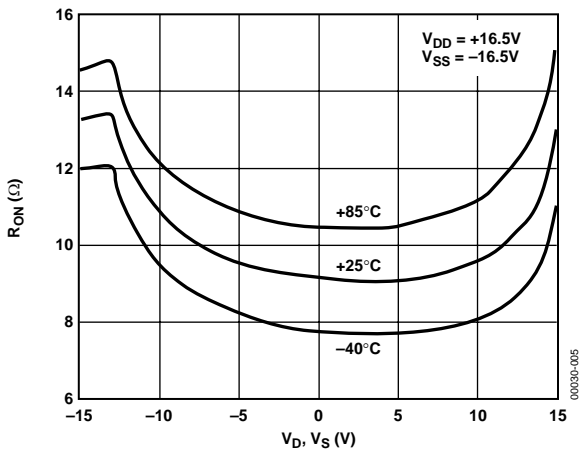


Figure 5. R_{ON} as a Function of $V_D (V_S)$ for Different Temperatures: Dual Supply

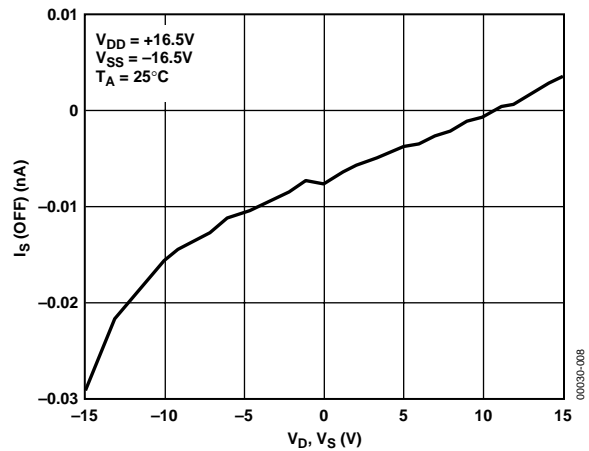


Figure 8. I_S (OFF) Leakage Current as a Function of $V_D (V_S)$: Dual Supply

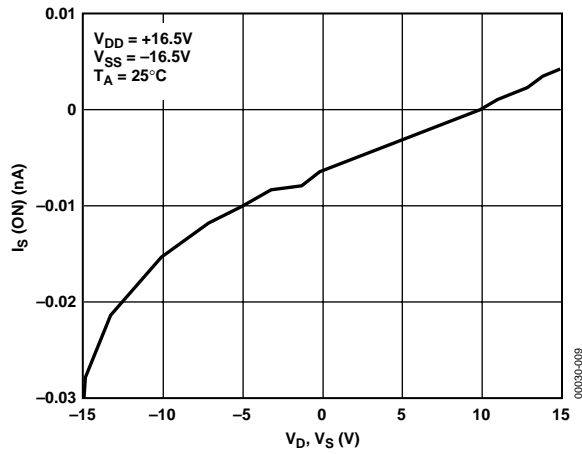


Figure 9. I_S (ON) Leakage Current as a Function of V_D (V_S): Dual Supply

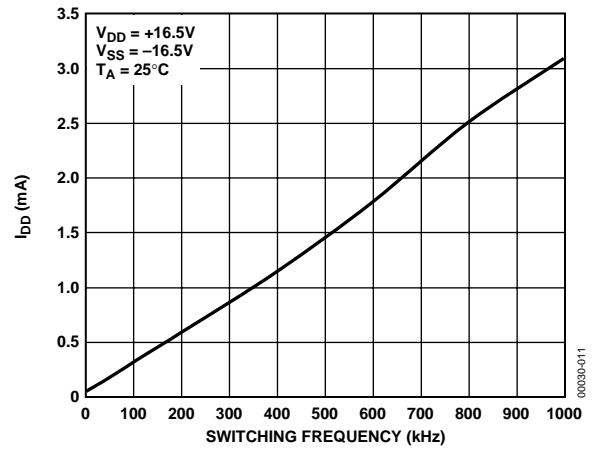


Figure 11. I_{DD} as a Function of Switching Frequency: Dual Supply

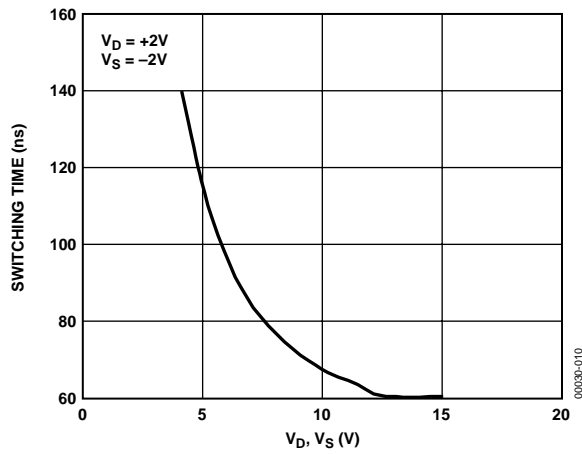


Figure 10. Switching Time as a Function of V_D (V_S): Dual Supply

TEST CIRCUITS

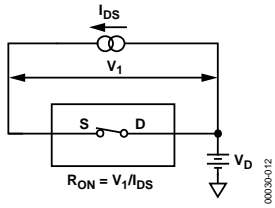


Figure 12. On Resistance

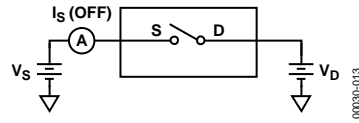


Figure 13. Off Leakage

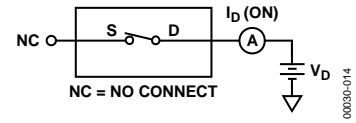


Figure 14. On Leakage

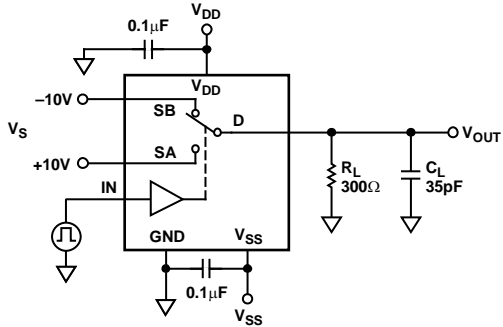


Figure 15. Switching Times

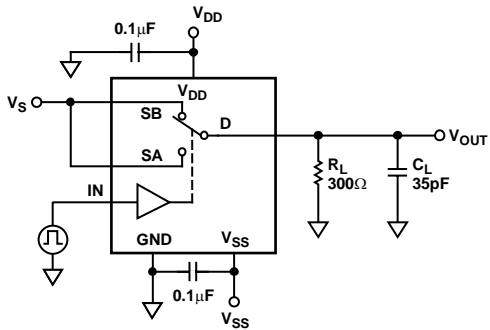
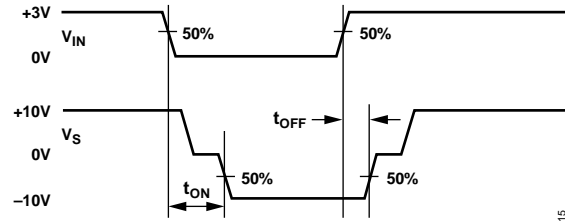


Figure 16. Break-Before-Make Delay, t_{open}

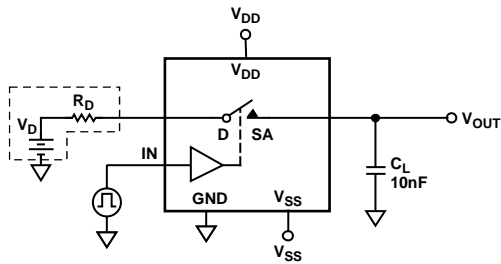
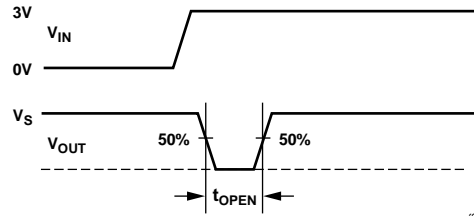


Figure 17. Charge Injection

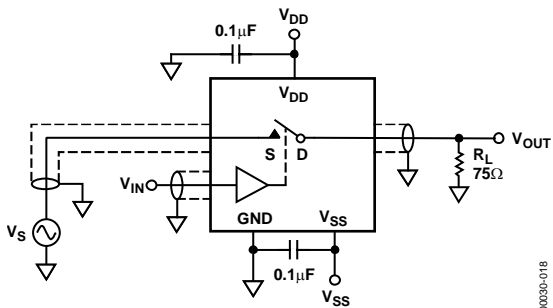
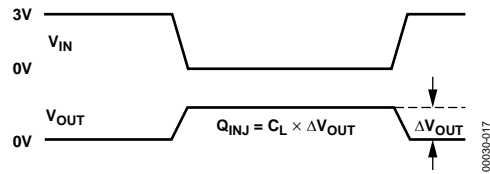


Figure 18. Off Isolation

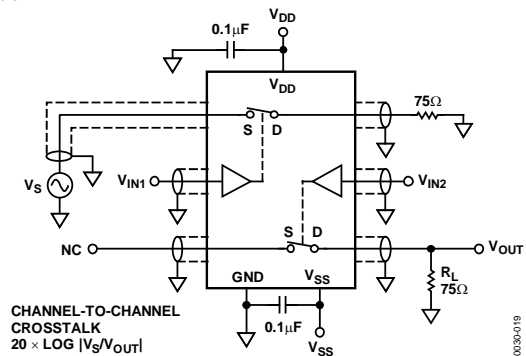


Figure 19. Channel-to Channel Crosstalk

APPLICATIONS INFORMATION

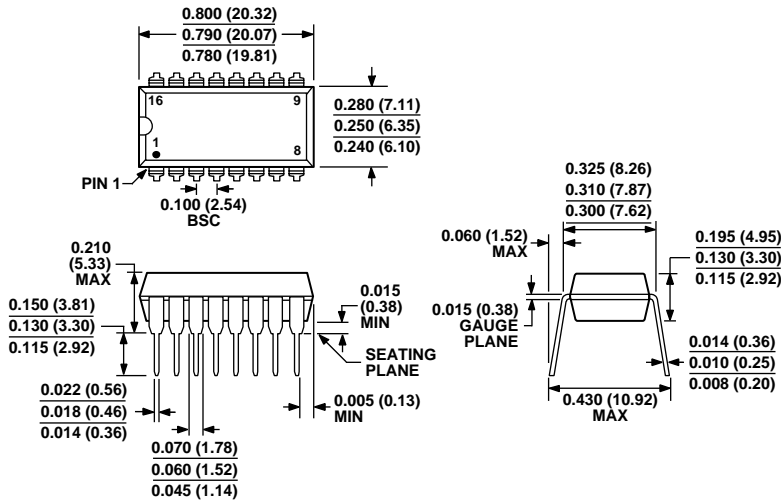
ADG436 SUPPLY VOLTAGES

The ADG436 can operate from a dual or single supply. V_{SS} should be connected to GND when operating with a single supply. When using a dual supply, the ADG436 can also operate with unbalanced supplies, for example $V_{DD} = 20\text{ V}$ and $V_{SS} = -5\text{ V}$. The only restrictions are that V_{DD} to GND must not exceed 30 V, V_{SS} to GND must not drop below -30 V , and V_{DD} to V_{SS} must not exceed +44 V. It is important to remember that the ADG436 supply voltage directly affects the input signal range, the switch on resistance and the switching times of the part. The effects of the power supplies on these characteristics can be clearly seen from the Typical Performance Characteristics curves.

POWER-SUPPLY SEQUENCING

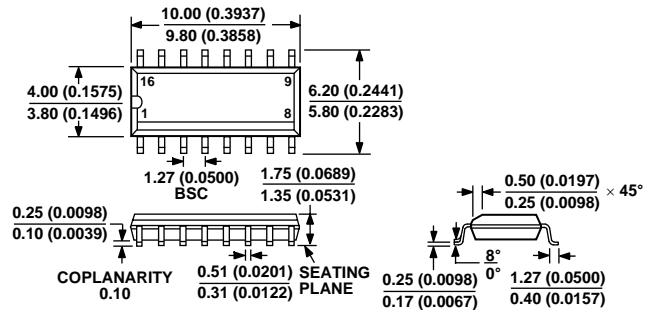
When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those listed in the Absolute Maximum Ratings. Always sequence V_{DD} on first followed by V_{SS} and the logic signals. An external signal can then be safely presented to the source or drain of the switch.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 20. 16-Lead Plastic Dual In-Line Package [PDIP] (N-16)
 Dimensions are shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 21. 16-Lead Narrow Body Standard Small Outline Package [SOIC] (R-16)
 Dimensions are shown in millimeters and (inches)

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|------------------------|-------------------|--------------------------------|----------------|
| ADG436BN | -40°C to +85°C | 16-Lead PDIP | N-16 |
| ADG436BNZ ¹ | -40°C to +85°C | 16-Lead PDIP | N-16 |
| ADG436BR | -40°C to +85°C | 16-Lead 0.15" Narrow Body SOIC | R-16 |
| ADG436BR-REEL | -40°C to +85°C | 16-Lead 0.15" Narrow Body SOIC | R-16 |
| ADG436BRZ | -40°C to +85°C | 16-Lead 0.15" Narrow Body SOIC | R-16 |
| ADG436BRZ-REEL | -40°C to +85°C | 16-Lead 0.15" Narrow Body SOIC | R-16 |

¹ Z = Pb-free part.