

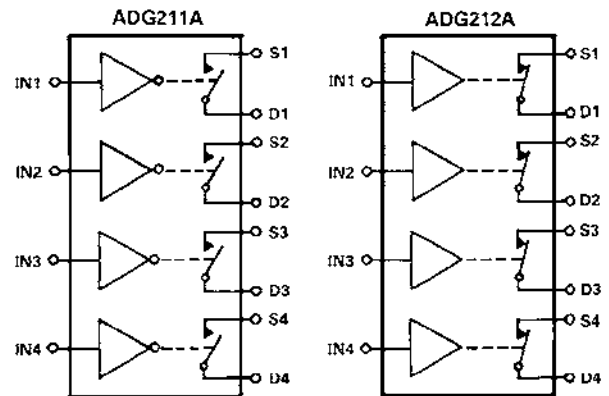
ADG211A/ADG212A
FEATURES

- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (115Ω max)
- Low Leakage (0.5nA typ)
- Break Before Make Switching
- Single Supply Operation Possible
- Extended Plastic Temperature Range
(-40°C to +85°C)
- TTL/CMOS Compatible
- Available in 16-Lead DIP/SOIC and
20-Lead PLCC Packages
- Superior Second Source:
ADG211A Replaces DG211
ADG212A Replaces DG212

GENERAL DESCRIPTION

The ADG211A and ADG212A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG211A and ADG212A consist of four SPST switches. They differ only in that the digital control logic is inverted. In multiplexer applications, all switches exhibit break-before-make switching action when driven simultaneously. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.



SWITCHES SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. **Extended Signal Range:**
These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. **Single Supply Operation:**
For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. **Low Leakage:**
Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG211A IN	ADG212A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table 1. Truth Table
REV. B

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ADG211A/ADG212A—SPECIFICATIONS ($V_{DD} = +15V$, $V_{SS} = -15V$, $V_L = 5V$, unless otherwise noted.)

Parameter	ADG211AKN ADG212AKN		Units	Test Conditions	
	25°C	-40°C to +85°C			
ANALOG SWITCH					
Analog Signal Range	± 15	± 15	Volts	$-10V \leq V_S \leq +10V$, $I_{DS} = 1mA$, Test Circuit 1	
R_{ON}	115	175	Ω_{max}		
R_{ON} vs. V_D (V_S)	20		% typ		
R_{ON} Drift	0.5		%/°C typ		
R_{ON} Match	5		% typ		
I_S (OFF)	0.5		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2	
OFF Input Leakage	5	100	nA max		
I_D (OFF)	0.5		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2	
OFF Output Leakage	5	100	nA max		
I_D (ON)	0.5		nA typ	$V_D = V_S = \pm 14V$; Test Circuit 3	
ON Channel Leakage	5	200	nA max		
DIGITAL CONTROL					
V_{INH} , Input High Voltage		2.4	V min	TTL Compatibility is Independent of V_L	
V_{INL} , Input Low Voltage		0.8	V max		
I_{INL} or I_{INH}		1	μA max		
C_{IN} , Digital Input Capacitance	5		pF typ		
DYNAMIC CHARACTERISTICS					
t_{OPEN}^1	30		ns typ	Test Circuit 4	
t_{ON}^1	600		ns max		Test Circuit 5
t_{OFF}^1	450		ns max		Test Circuit 5
OFF Isolation	80		dB typ	$V_S = 10V(p-p)$; $f = 100kHz$ $R_L = 75\Omega$; Test Circuit 6	
Channel-to-Channel Crosstalk	80		dB typ	Test Circuit 7	
C_S (OFF)	5		pF typ	$R_S = 0\Omega$; $C_L = 1000pF$; $V_S = 0V$ Test Circuit 8	
C_D (OFF)	5		pF typ		
C_S, C_D (ON)	16		pF typ		
Q_{INJ} , Charge Injection	20		pC typ		
POWER SUPPLY					
I_{DD}	0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}	
I_{DD}	1		mA max		
I_{SS}	0.1		mA typ		
I_{SS}	0.2		mA max		
I_L	0.9		mA max		

NOTE

¹Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

ADG211A/ADG212A

ABSOLUTE MAXIMUM RATINGS*

($T_A = 25^\circ\text{C}$ unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DI} to GND	25V
V_{SS} to GND	-25V
V_L to GND	-0.3V, 25V
Analog Inputs ¹	
Voltage at S, D	$V_{SS} - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA

Digital Inputs¹

Voltage at IN	$V_{SS} - 2\text{V}$ to $V_{DD} + 2\text{V}$ or 20mA, Whichever Occurs First
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Power Dissipation (Any Package)

Up to $+75^\circ\text{C}$	470mW
Derates above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$
Operating Temperature	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

NOTE

¹Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

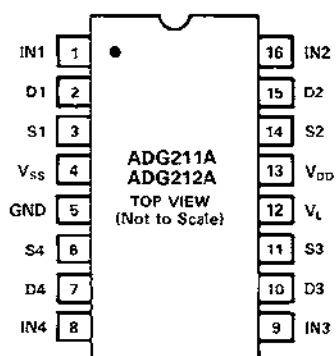
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

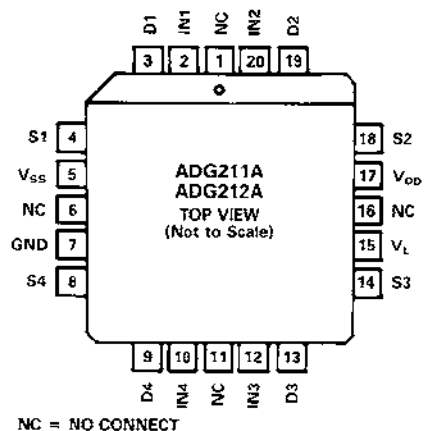


PIN CONFIGURATIONS

DIP, SOIC



PLCC



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG211AKN	-40°C to $+85^\circ\text{C}$	N-16
ADG211AKR	-40°C to $+85^\circ\text{C}$	R-16A
ADG211AKP	-40°C to $+85^\circ\text{C}$	P-20A
ADG212AKN	-40°C to $+85^\circ\text{C}$	N-16
ADG212AKR	-40°C to $+85^\circ\text{C}$	R-16A
ADG212AKP	-40°C to $+85^\circ\text{C}$	P-20A

*N = Plastic DIP; R = 0.15" Small Outline IC (SOIC);
P = Plastic Leaded Chip Carrier (PLCC).

ADG211A/ADG212A—Typical Performance Characteristics

The switches can comfortably operate anywhere in the 10V to 15V single or dual supply range, with only a slight degradation in performance. The following graphs show the relevant performance curves. The test circuits and test conditions are given in a following section, "Test Circuits."

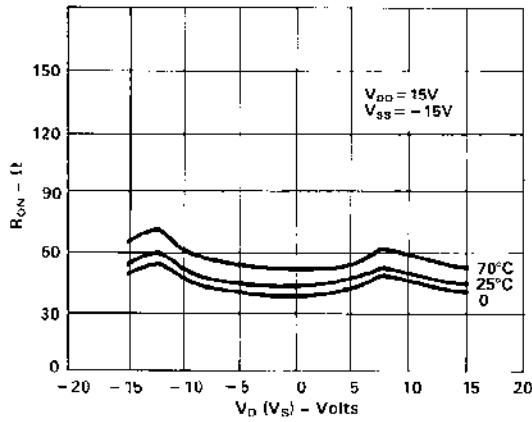


Figure 1. R_{ON} as a Function of $V_D (V_S)$: Dual ± 15 Supplies

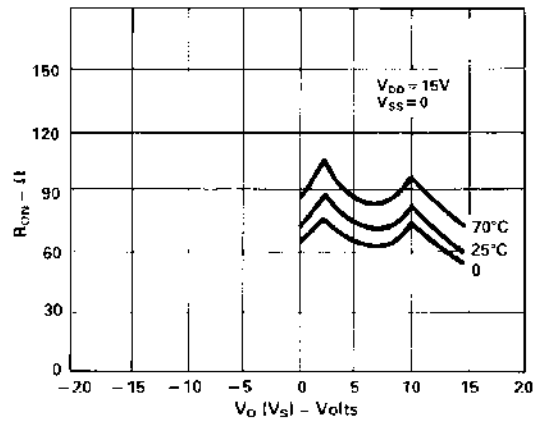


Figure 2. R_{ON} as a Function of $V_D (V_S)$: Single + 15V Supply

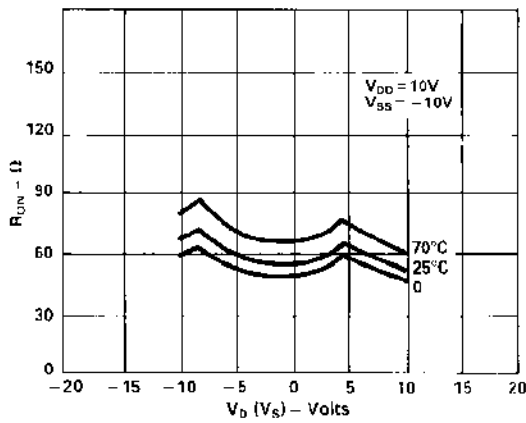


Figure 3. R_{ON} as a Function of $V_D (V_S)$: Dual ± 10 V Supplies

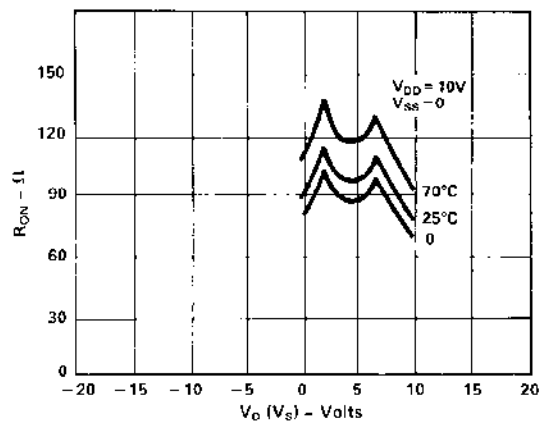


Figure 4. R_{ON} as a Function of $V_D (V_S)$: Single + 10V Supply

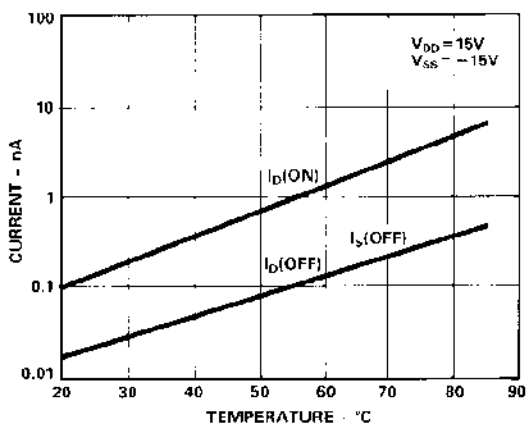


Figure 5. Leakage Current as a Function of Temperature (Note: Leakage Current Reduces as the Supply Voltages Reduce)

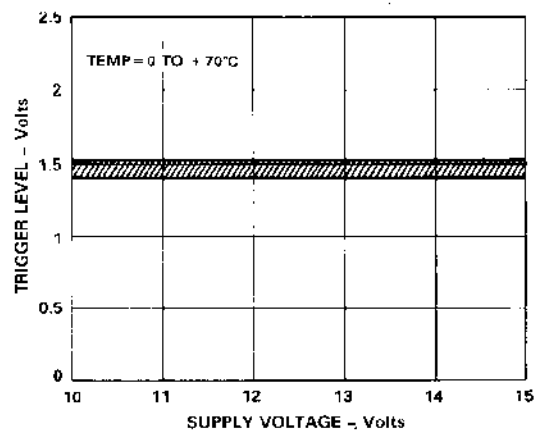


Figure 6. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply Voltage

Typical Performance Characteristics—ADG211A/ADG212A

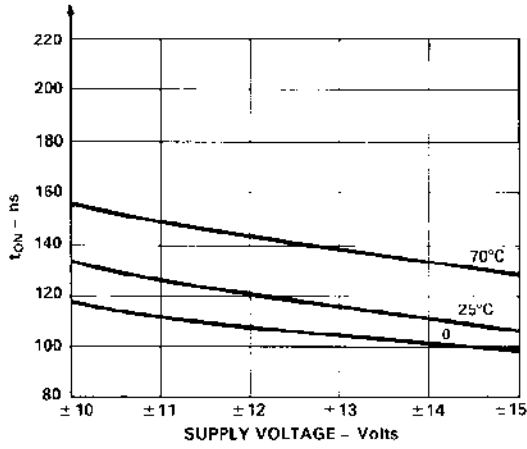


Figure 7. t_{ON} vs. Supply Voltage, (Dual Supply)

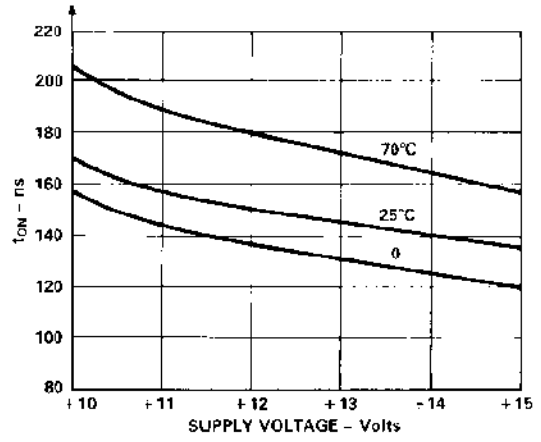


Figure 8. t_{ON} vs. Supply Voltage, (Single Supply)

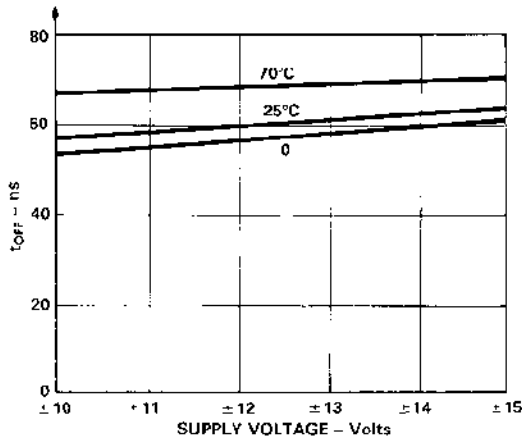


Figure 9. t_{OFF} vs. Supply Voltage, (Dual Supply)

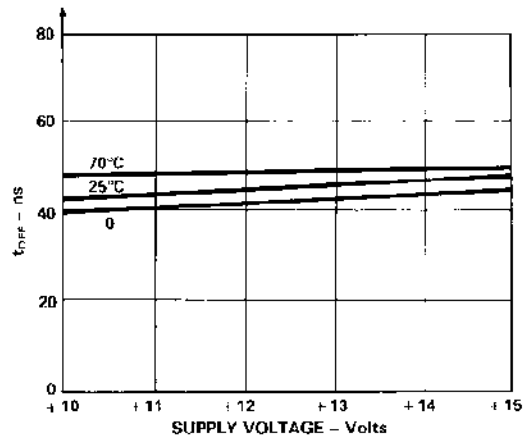


Figure 10. t_{OFF} vs. Supply Voltage, (Single Supply)

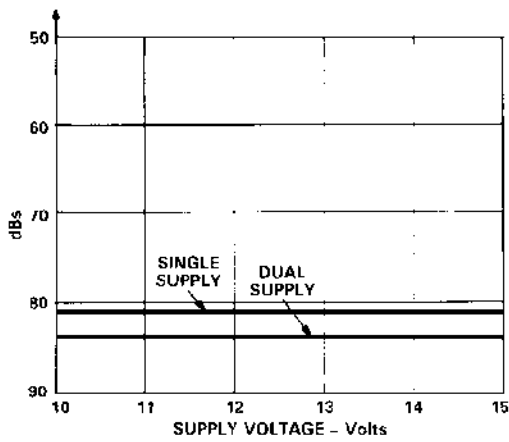


Figure 11. Off Isolation and Channel-to-Channel Crosstalk vs. Supply Voltage

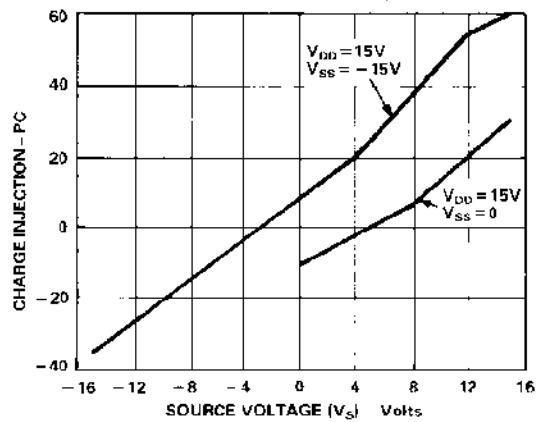


Figure 12. Charge Injection vs. Source Voltage (V_S) for Dual and Single 15V Supplies

ADG211A/ADG212A—Typical Performance Characteristics

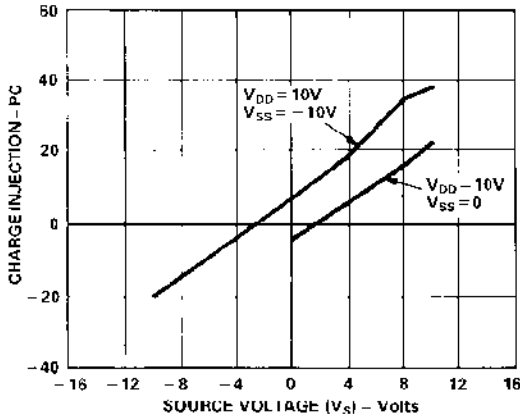


Figure 13. Charge Injection vs. Source Voltage for Dual and Single 10V Supplies

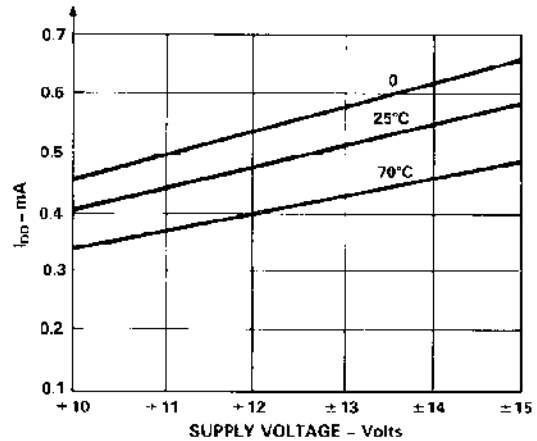


Figure 14. I_{DD} vs. Supply Voltage, (Dual Supply)

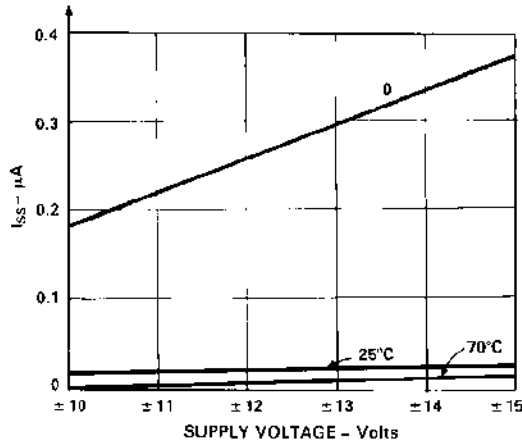


Figure 15. I_{SS} vs. Supply Voltage, (Dual Supply)

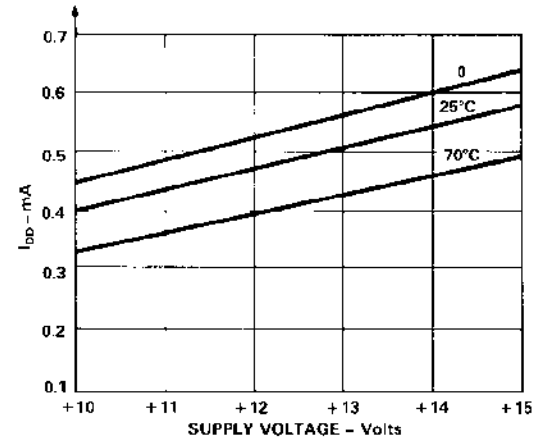


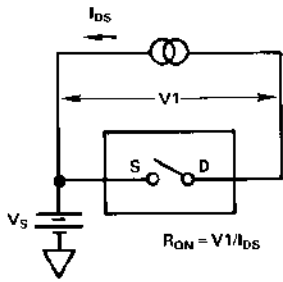
Figure 16. I_{DD} vs. Supply Voltage, (Single Supply)

TERMINOLOGY

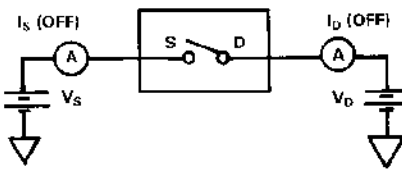
R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition

t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INH}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
V_L	Logic supply voltage
I_{DD}	Positive supply current
I_{SS}	Negative supply current

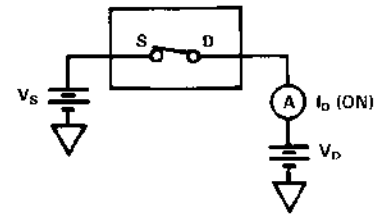
Test Circuits—ADG211A/ADG212A



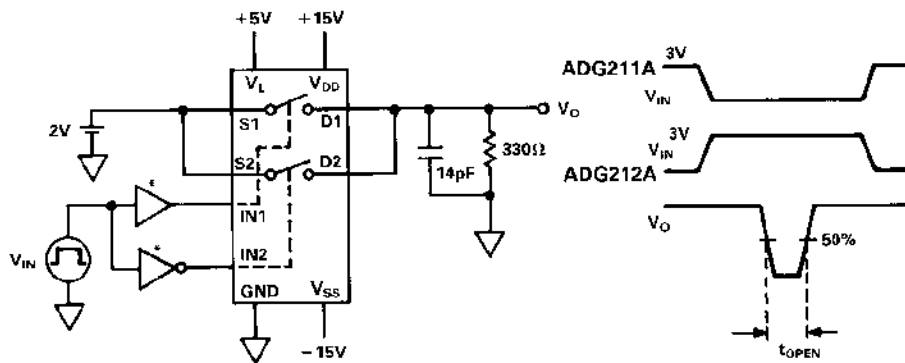
Test Circuit 1



Test Circuit 2

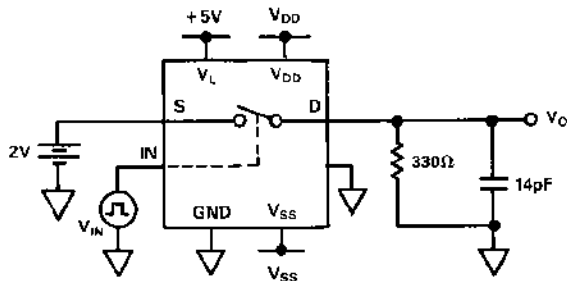


Test Circuit 3

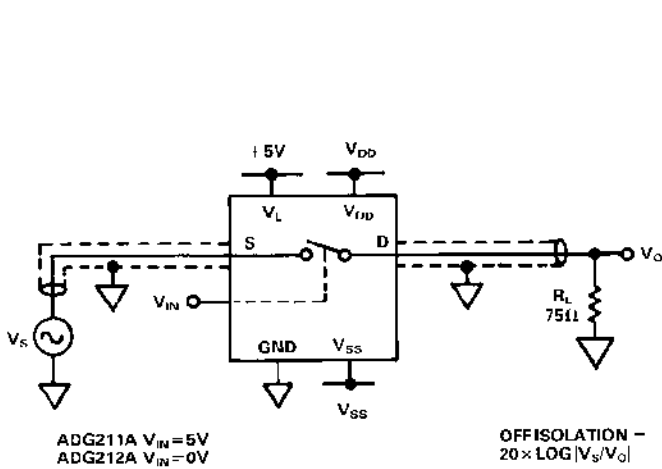


*BOTH THE BUFFER AND INVERTER SHOULD HAVE THE SAME PROPAGATION DELAY.

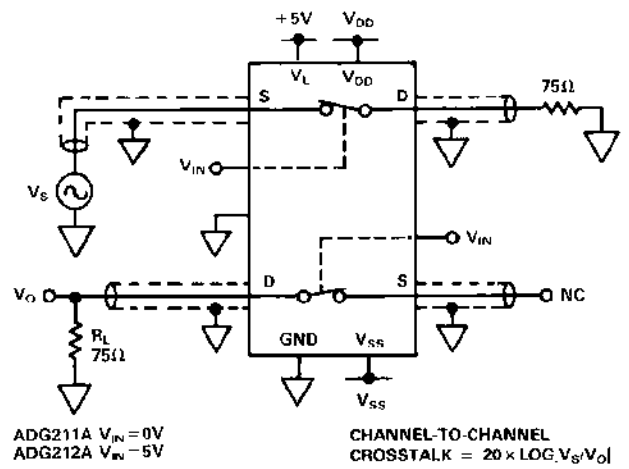
Test Circuit 4



Test Circuit 5

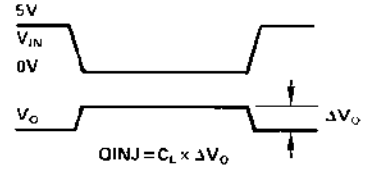
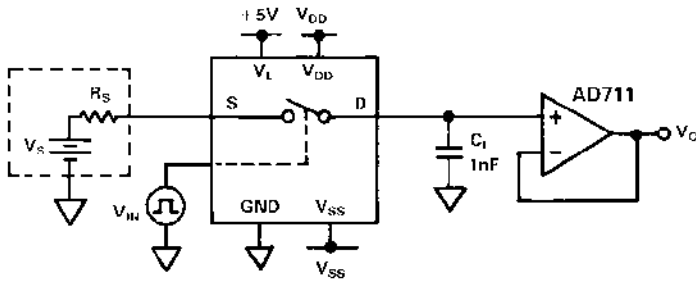


Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk

ADG211A/ADG212A

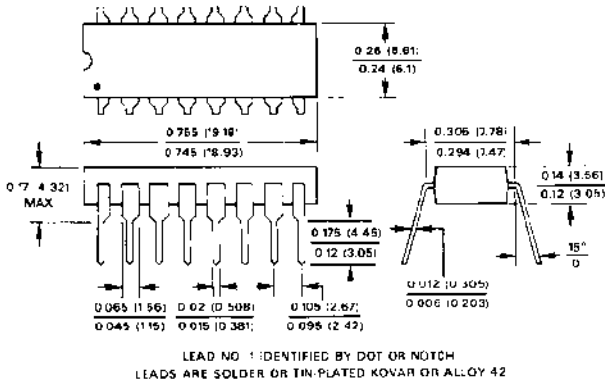


Test Circuit 8. Charge Injection

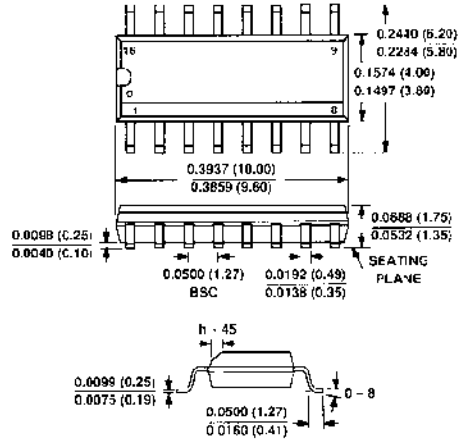
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic (N-16)



16-Lead Narrow Body SOIC (R-16A)



20-Terminal Plastic Leaded Chip Carrier (P-20A)

