ANALOG DEVICES

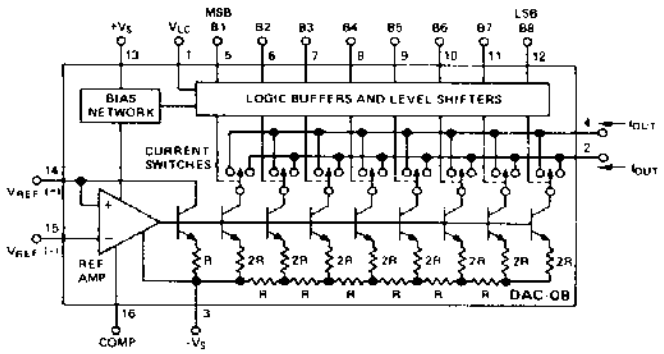
8-Bit Monolithic High Speed Multiplying D/A Converter

AD DAC-08

FEATURES

- Exact Replacement for Industry Standard DAC-08
- Fast (85ns typical) Settling Time
- Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
- Wide Output Voltage Compliance: -10V to +18V
- Single Chip Monolithic Construction

AD DAC-08 FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD DAC-08 is a low-cost, 8-bit monolithic multiplying digital-to-analog converter featuring typical settling times of 85ns. The chip contains 8 matched bipolar current steering switches, a precision resistor network, and high-speed control amplifier, thus integrating all important circuit functions on a single chip.

The AD DAC-08 provides matching of full-scale output current to the reference current within 1LSB. Analog Devices' precision linear processing makes this matching possible without the use of laser trimming. Diffused resistors are used rather than thin-film resistors in order to provide specified performance at low cost.

The AD DAC-08 is recommended for use in applications requiring 8-bit accuracy and fast settling times coupled with ease of use. The AD DAC-08 also provides an alternate source for designs already using the standard DAC-08.

The AD DAC-08 is available in 5 performance grades: the AD DAC-08A and AD DAC-08 are rated for the -55°C to +125°C extended temperature range; and the AD DAC-08H, E, and C grades are specified for the 0 to +70°C commercial temperature range. All models are guaranteed monotonic over their full temperature range, and all are packaged in a hermetically-sealed 16-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD DAC-08 is a true second-source equivalent to the industry standard DAC-08.
2. The versatile current-in, current-out design, choice of fixed or variable reference, and CMOS or TTL compatible inputs offer the user greater flexibility in applying the device.
3. The fast settling time allows the AD DAC-08 to be used in applications such as CRT displays, waveform generators, and high-speed analog-to-digital converters.
4. The high impedance current output can drive a resistor directly, or be used with an external op amp to produce a low impedance output voltage.
5. The AD DAC-08 is available in chip form for use in hybrid microcircuits. Consult the chip section for available grades and application details.

SPECIFICATIONS

The AD DAC-08 and AD DAC-08A specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = -55°C$ to $+125°C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08 MIN	AD DAC-08 TYP	AD DAC-08 MAX	AD DAC-08A MIN	AD DAC-08A TYP	AD DAC-08A MAX	UNITS
RESOLUTION					8			8	Bits
MONOTONICITY		$T_A = -55°C$ to $+125°C$		GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = -55°C$ to $+125°C$			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	135		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$ typ	−10		+18	−10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, R_{15} = 5.000kΩ; $T_A = 25°C$	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	V− = −5.0V	0	2.0	2.1	0	2.0	2.1	mA
		V− = −7.0 to −18V	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$							
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		−2.0	−10		−2.0	−10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	V− = −15V	−10		+18	−10		+18	V
LOGIC THRESHOLD RANGE	V_{THR}	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V− = 4.5V to −18V		±0.002	±0.01		±0.002	±0.01	%/%
		$I_{REF} = 1.0mA$							
POWER SUPPLY CURRENT									
From $+V_S$	I_+		0.4	2.3	3.8	0.4	2.3	3.8	mA
From $-V_S$	I_-		−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48	mW
		+5V, −15V, $I_{REF} = 2.0mA$		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08D			AD DAC-08AD		

NOTES
[1] See Section 19 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- AD DAC-08, DAC-08A. . . . . −55°C to +125°C
- AD DAC-08E, C, H . . . . . 0 to +70°C

Storage Temperature . . . . . −65°C to +150°C
- Power Dissipation 500mW
- Above 100°C Derate by . . . . . 10mW/°C

Lead Soldering Temperature . . . . . 300°C (60sec)
$-V_S$ Supply to $+V_S$ Supply 36V
Logic Inputs. . . . . $-V_S$ to $(-V_S + 36V)$
- V_{LC} . . . . . $-V_S$ to $+V_S$

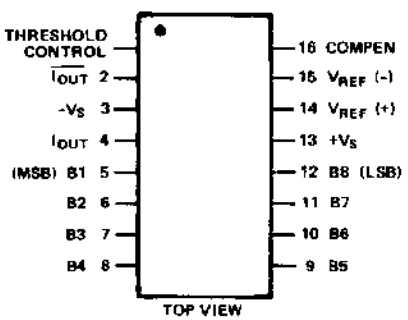
Reference Inputs (V_{14}, V_{15}). . . . . $-V_S$ to $+V_S$
Reference Input Differential
- Voltage (V_{14} to V_{15}). . . . . ±18V

Reference Input Current (I_{14}) 5.0mA

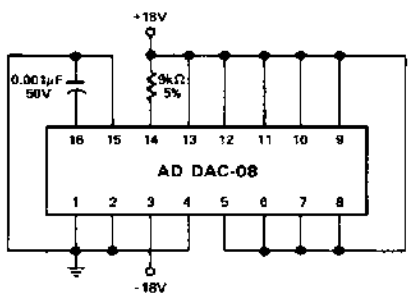
SPECIFICATIONS

The AD DAC-08C, E, and H specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 0$ to $+70^\circ C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08C MIN	AD DAC-08C TYP	AD DAC-08C MAX	AD DAC-08E MIN	AD DAC-08E TYP	AD DAC-08E MAX	AD DAC-08H MIN	AD DAC-08H TYP	AD DAC-08H MAX	UNITS
RESOLUTION					8			8			8	Bits
MONOTONICITY		$T_A = 0$ to $+70^\circ C$		GUARANTEED			GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = 0$ to $+70^\circ C$			±0.39			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	150		85	150		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±80		±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$	-10		+18	-10		+18	-10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, $R_{15} = 5.000k\Omega$; $T_A = 25^\circ C$	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±2.0	±16		±1.0	±8.0		±0.5	±4.0	µA
ZERO SCALE CURRENT	I_{ZS}			0.2	4.0		0.2	2.0		0.1	1.0	µA
OUTPUT CURRENT RANGE	I_{FSR}	V- = -5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V- = -7.0 to -18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS												
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$-10V \le V_{IN} \le +0.8V$		-2.0	-10		-2.0	-10		-2.0	-10	µA
Logic "1"	I_{IH}	$2.0V \le V_{IN} \le 18V$		0.002	10		0.002	10		0.002	10	µA
LOGIC INPUT SWING	V_{IS}	V- = -15V	-10		+18	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{THR}	$V_S = \pm 15V$	-10		+13.5	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	µA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		4.0	8.0		mA/µs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V; $I_{REF} = 1.0mA$		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%/%
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8	0.4	2.3	3.8	0.4	2.3	3.8	mA
	I-	From $-V_S$	-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48		33	48	mW
		+5V, -15V, $I_{REF} = 2.0mA$		108	136		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08CD			AD DAC-08ED			AD DAC-08HD		



Pin Connections



Burn-In Circuit

APPLYING THE AD DAC-08

Reference Connections

Figure 1 shows the block diagram of the AD DAC-08 circuit. A reference current (equal to the desired full-scale output current) is applied to pin 14. The reference amplifier adjusts the base voltage of the NPN current source transistors. The collector currents are binarily weighted, and their sum is equal to 255/256 times the reference current. The binary weighting is accomplished by the diffused resistor R-2R ladder network. The individual collector currents are steered into either the I_{OUT} or $\overline{I_{OUT}}$ lines by the current switches. These switches are driven by level shifters which can accept TTL or CMOS logic levels directly. The I_{OUT} and $\overline{I_{OUT}}$ lines can drive an op amp summing junction or can drive resistive loads directly due to the wide range of output compliance voltage.

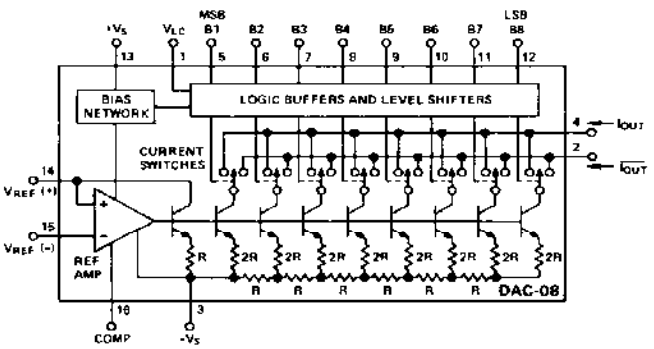
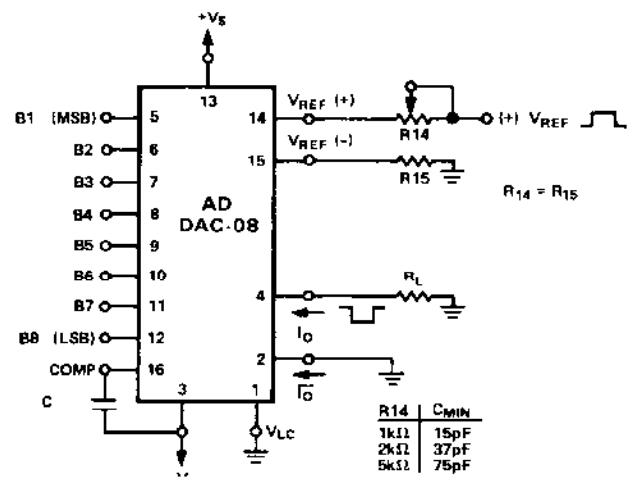


Figure 1. AD DAC-08 Block Diagram

Figure 2 illustrates the connections for positive and negative references. When a positive reference is used (Figure 2a), resistor R14 (equal to V_{REF} divided by the desired I_{FS}) establishes the reference current into pin 14. Reference amplifier bias current errors are minimized by connecting R15 (equal to R14) from pin 15 to ground. Adjustment of the output scale can be done by trimming R14, although in most applications the tight initial matching between reference current and output current will be adequate.



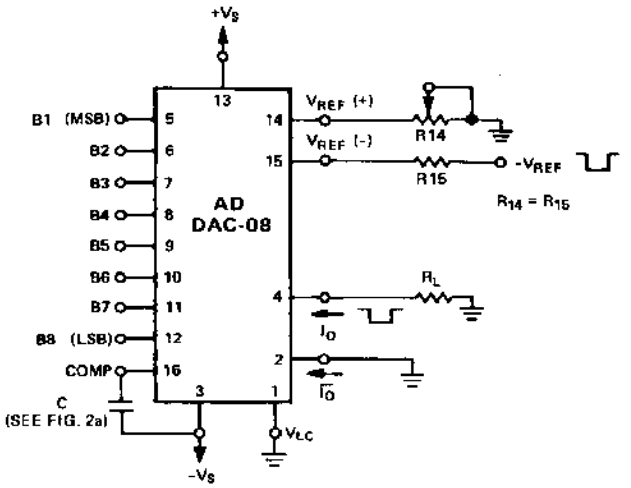


Figure 2b. Connections for Use with Negative Reference

of bias current cancellation only and need not be a precision resistor. Note that the input impedance for a negative reference is very high, while a positive reference sees an impedance equal to R14.

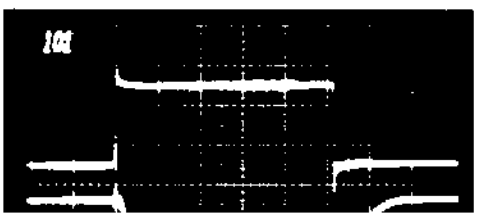
When a dc reference is used, a 0.01μF reference bypass capacitor is recommended. The reference should be a low-drift, well-regulated and filtered type, such as the AD581 10V reference IC. Other values of reference voltage may be used, provided that R14 is chosen for a reference current between 0.2mA and 4.0mA.

MULTIPLYING MODE PERFORMANCE

The AD DAC-08 can be used to perform two-quadrant digital-analog multiplication by applying an ac reference signal. When an ac reference is used, pin 15 must be offset to insure that pin 14 is always at a higher potential than pin 15.

The reference amplifier must be properly compensated in ac applications to insure stability. The value of the capacitor from pin 16 to $-V_S$ depends on the value of R14. Minimum values of compensation capacitor for R14 values of 1, 2 and 5kΩ are 15, 37 and 75pF respectively.

For fastest response to a pulsed reference, low values of R14 should be used, allowing smaller values of compensation capacitor. It is possible to lower the equivalent resistance at pin 14 by connecting a shunt resistor to ground. Figure 3 shows the performance with equivalent resistance of 200Ω and no compensation capacitor. Slew rate is approximately 15mA/μs under these conditions.



Typical Performance Photographs

The photographs on this page demonstrate the dynamic performance of the AD DAC-08. The AD DAC-08 is capable of extremely fast settling time, typically 85 nanoseconds for a full-scale step with I_{REF} = 2.0mA. As with any high speed circuitry, component layout must be optimized for minimum parasitic capacitances if full speed is to be realized.

Figure 4 below shows the output settling characteristic for a full-scale step. The vertical scale is 1LSB per division. Note that the zero-to-full scale settling time (Figure 4a) to within 1/2LSB is approximately 70 nanoseconds.

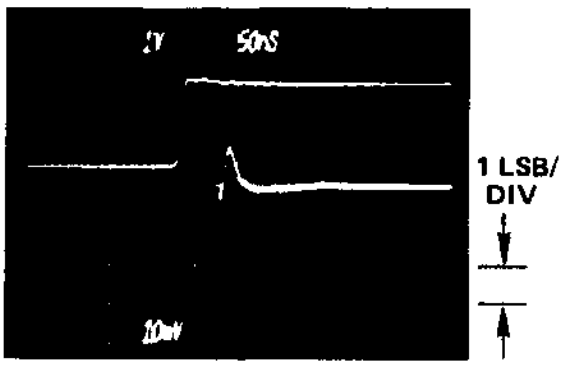


Figure 4a. Zero to Full-Scale Settling

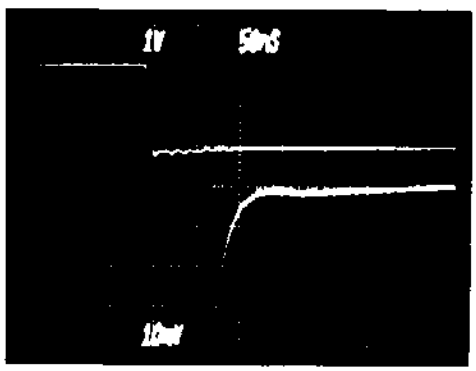


Figure 4b. Full-Scale to Zero Settling

Since the settling time of a DAC circuit includes propagation delay, slewing time, and final settling, switching time is best measured when only the LSB is switched. This minimizes the slewing time necessary. The LSB switching characteristic is shown in Figure 5.

SETTLING TIME MEASUREMENT

It should be noted that settling time measurement is not a simple matter. Since 1/2LSB of a 2.0mA full scale is only 4μA, a 1kΩ load resistance is needed to provide adequate drive for most oscilloscopes. However, any stray capacitance can cause the settling time of the fixture to be longer than the DAC settling time. For example, 15pF stray capacitance can cause a settling time to 1/2LSB of nearly 100 nanoseconds in the test fixture alone. The circuit of Figure 6 reduces the capacitance at the measurement node to less than 5pF, allowing more accurate determination of settling time.

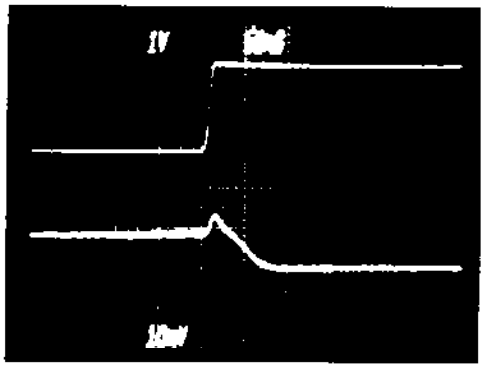


Figure 5. LSB Switching

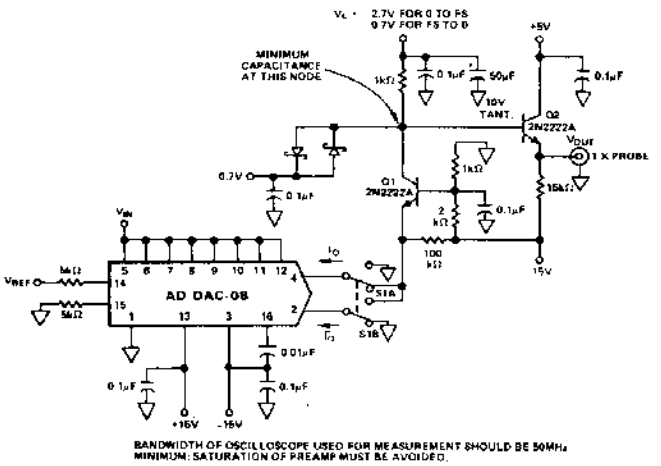


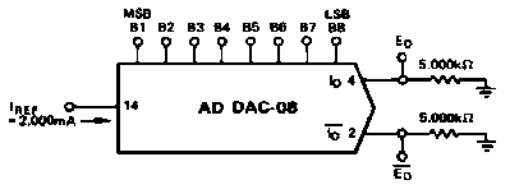
Figure 6. Settling Time Test Circuit

LOGIC INPUT CIRCUIT

The AD DAC-08 digital inputs will accommodate all popular logic families. The switching threshold is adjustable by applying a voltage to the logic threshold control pin (pin 1). The threshold is nominally 1.4 volts above V_{LC} at room temperature. For TTL/DTL interface, pin 1 is simply grounded. The logic inputs will tolerate wide voltage swings; for example, for $-V_S$ = −15V, the inputs may swing between −10V and +18V.

OUTPUT CONNECTIONS

The I_O and $\overline{I_O}$ outputs provide the user with several possible output configurations. Current is steered into the I_O terminal when a bit is at Logic "1", and into $\overline{I_O}$ when the bit is at Logic "0". Either output may be used, or both may be used simultaneously. If only one output is used, the unused output must still be connected to ground or some other point capable of sourcing I_{FS}.



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
FULL SCALE -LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
HALF SCALE -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

Figure 7. High Impedance Voltage Output

The wide output compliance range permits the AD DAC-08 to drive a resistive load directly. For example, with I_{REF} = 2.0mA, and a 5kΩ resistor from pin 4 to ground, the voltage at pin 4 varies from 0V with all bits OFF to -9.960V with all bits ON. While this is the simplest current-to-voltage conversion, it presents a 5kΩ output impedance, which adversely affects settling time and requires buffering.

An operational amplifier configured as a current-to-voltage converter will lower the output impedance and provide a voltage inversion. An output range of zero to +9.960V is then produced with a 5kΩ feedback resistor as shown in Figure 8.

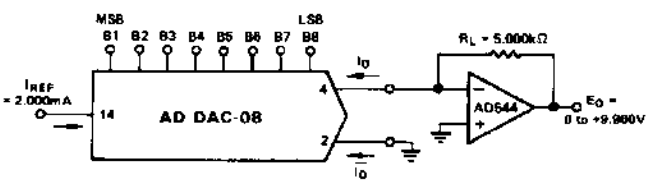
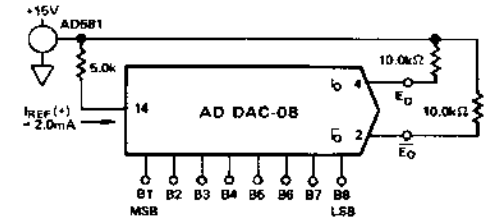


Figure 8. Low Impedance Voltage Output

Bipolar output voltage ranges are also possible. Figure 9 demonstrates the simplest scheme, providing a -9.92 to +10.00 volt scale in 80 millivolt steps. The voltage output has a high impedance as shown and should be buffered with an amplifier connected as a voltage follower.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	- 9.920	+10.000
POS FULL SCALE -LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE -LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

Figure 9. Bipolar Voltage Output