ANALOG DEVICES

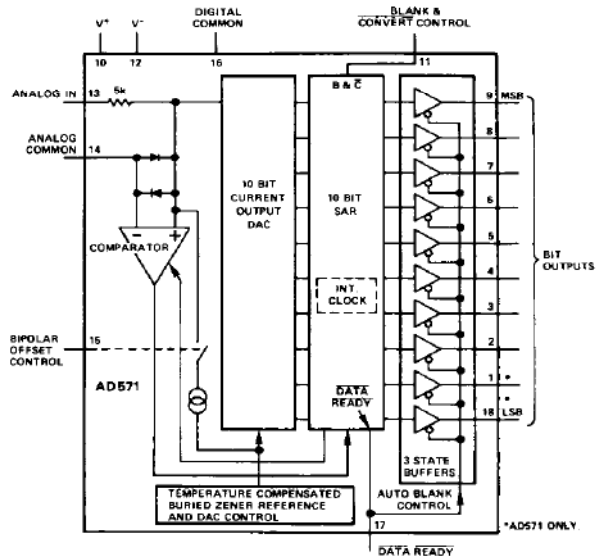
8- and 10-Bit Analog-to-Digital Converters

AD570/AD571*

FEATURES

Complete A/D Converters with Reference and Clock
AD570: 8 Bit
AD571: 10 Bit
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD570/AD571 are successive approximation A/D converters consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform full accuracy conversions in 25μs.

The AD570/AD571 incorporate advanced integrated circuit design and processing technologies. They employ I^2L (integrated logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and −15V, the AD570/AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three-state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ high blanks the outputs and readies the device for the next conversion.

The devices are available in two versions: the "J" and "K" specified for the 0 to +70°C temperature range. The "S" guarantees the specified accuracy and no missing codes from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. The AD570 is an 8-bit version which employs the same architecture. No external components are required to perform a conversion.
2. The AD570/AD571 are single chip devices employing advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The converters accept either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
4. Each device offers the specified accuracy with no missing codes over its entire operating temperature range.
5. Operation is guaranteed with −15V and +5V to +15V supplies. The devices will also operate with a −12V supply.
6. The AD570 and AD571 are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

*Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.

AD570/AD571 — SPECIFICATIONS (T_A = +25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD570J Min	AD570J Typ	AD570J Max	AD570S Min	AD570S Typ	AD570S Max	Units
RESOLUTION[1]			8			8	Bits
RELATIVE ACCURACY							
T_{min} to T_{max}			±1/2			±1/2	LSB
FULL-SCALE CALIBRATION		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR ZERO			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY							
T_{min} to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full-Scale Calibration			±2			±2	LSB
POWER SUPPLY REJECTION							
CMOS Positive Supply							
+13.5V≤V+≤+16.5V	–	–	–	–	–	–	LSB
TTL Positive Supply							
+4.5V≤V+≤+5.5V			±2			±2	LSB
Negative Supply							
−16.0V≤V−≤−13.5V			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current							
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	µA
LOGIC INPUTS							
Input Current			±100			±100	µA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME							
T_{min} to T_{max}	15	25	40	15	25	40	µs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−12.0	−15	−16.5	−12.0	−15	−16.5	V
OPERATING CURRENT							
V+		7	10		7	10	mA
V−		9	15		9	15	mA
PACKAGE OPTION[2, 3]							
Ceramic (D-18)		AD570JD			AD570SD		

NOTES

[1]The AD570 is a selected version of the AD571 10-bit A-to-D converter. Only TTL logic inputs should be connected to Pins 1 and 18 (or no connection made) or damage may result.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION			10			10			10	Bits
RELATIVE ACCURACY, T_A			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL-SCALE CALIBRATION		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR ZERO			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full-Scale Calibration			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	–	–	–			±1	–	–	–	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−16.0V≤V−≤−13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[1]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	2.0			2.0			2.0			V
Logic "0"			0.8			0.8			0.8	V
CONVERSION TIME										
T_{min} to T_{max}	15	25	40	15	25	40	15	25	40	μs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+16.5	+4.5	+5.0	+7.0	V
V−	−12.0	−15	−16.5	−12.0	−15	−16.5	−12.0	−15	−16.5	V
OPERATING CURRENT										
V+		7	10		7	10		7	10	mA
V−		9	15		9	15		9	15	mA
PACKAGE OPTION[2,3]										
Ceramic (D-18)		AD571JD			AD571KD			AD571SD		

NOTES

[1]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[2]D = Ceramic DIP. For outline information see Package Information section.

[3]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices Military Products databook or current /883B data sheet.

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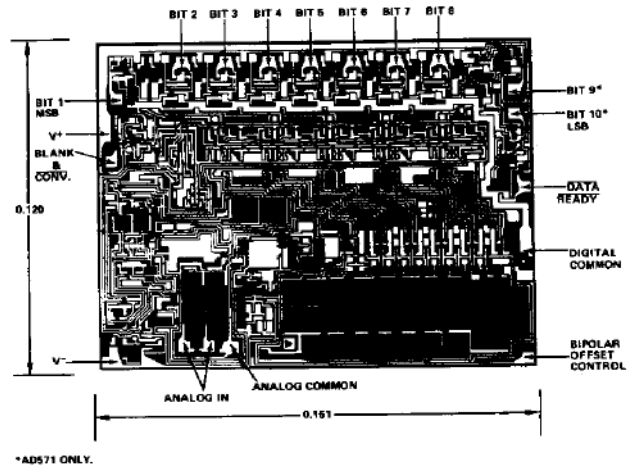
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD570J, S/AD571J, S	0 to +7V
AD571K	0 to +16.5V
V− to Digital Common	0 to −16.0V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

CHIP BONDING DIAGRAM



CIRCUIT DESCRIPTION

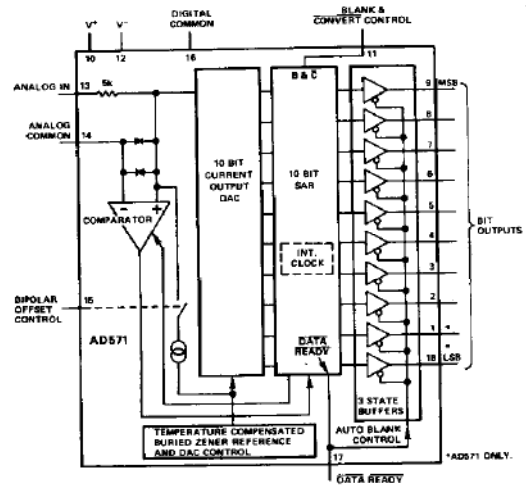
The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive approximation analog-to-digital conversion function. The AD570 is an 8-bit version. A functional block diagram of the AD570/AD571 is shown below. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit (AD571) current output DAC is sequenced by the I^2L successive approximation register (SAR) from its most-significant bit (MSB) to least-significiant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2LSB (0.05%).

Upon completion of the sequences, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further on.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows a positive bipolar offset current to be injected into the summing (+) node of the comparator to offset the DAC output. The nominal 0 to +10V unipolar input range now becomes a −5V to +5V range. The 5kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

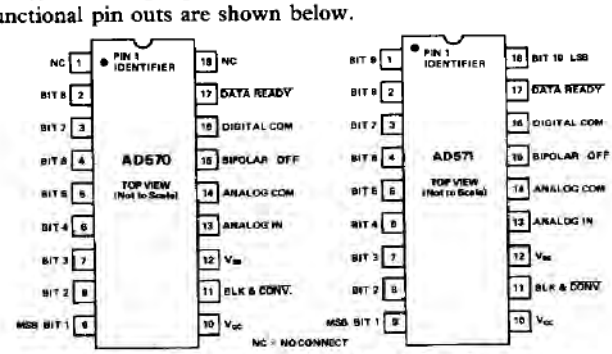
The AD570/AD571 are designed for optimum performance using a +5V and −15V supply, for which the J and S grades are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic.



AD570/AD571 Functional Block Diagram

CONNECTING THE AD570/AD571 FOR STANDARD OPERATION

The AD570/AD571 contain all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. The functional pin outs are shown below.



AD570 Pin Connections *AD571 Pin Connections*

FULL-SCALE CALIBRATION

The 5kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC when a full-scale analog input voltage of 10 volts – 1LSB is applied at the input. The input resistor is trimmed in this way so that if a fine-trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.990 (9.961 for the AD570) volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to Pin 13. Typical full-scale calibration error will then be about ±2LSB. If the more precise calibration is desired, a trimmer should be used instead. A 50Ω potentiometer should be used with the AD571 and a 200Ω with the AD570. Set the analog input at full scale and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of $10V/2^N$ (where N = number of bits).

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5V to +5V range with an offset binary code. The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 1.

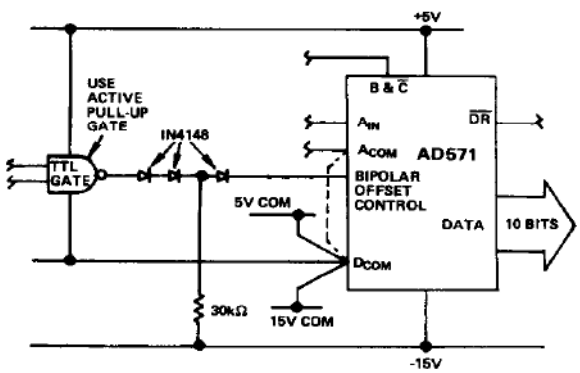


Figure 1. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON-MODE RANGE

The AD570/AD571 provide separate analog and digital common connections. The circuit will operate properly with as much as ±200mV of common-mode range between the two commons. This permits more flexible control of system common bussing and digital and analog return.

In normal operation the analog common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into analog common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The analog common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

ZERO OFFSET

The apparent zero point of the AD570/AD571 can be adjusted by inserting an offset voltage between the analog common of the device and the actual signal return or signal common. Figure 2 illustrates two methods of providing this offset for the AD571. Figure 2a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

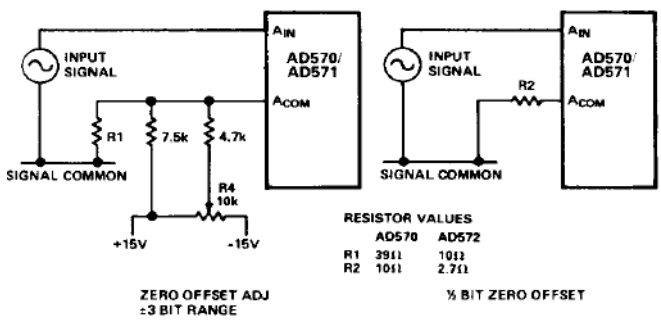


Figure 2a. *Figure 2b.*

Figure 3 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 2b. At balance

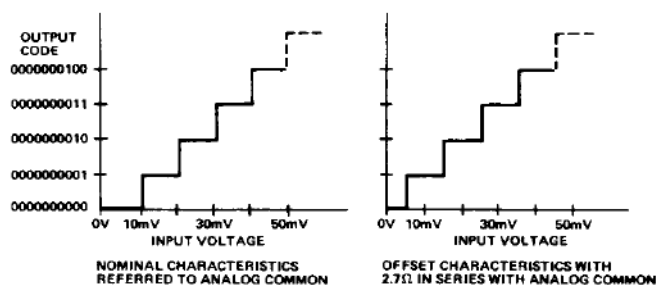


Figure 3. AD571 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights~9.755mV)

(after a conversion) approximately 2mA flows into the analog common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2mA analog common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2LSB is introduced, full-scale trimming as previously described should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the analog common terminal will disturb the offset voltage. Capacitive

decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A −5.0 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve for the AD571 is shown in Figure 4. The MSB transition for both the AD570 and the AD571 occurs at a −4.88mV input.

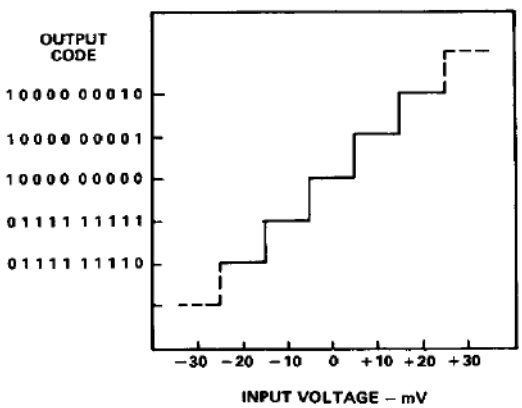


Figure 4. AD571 Transfer Curve – Bipolar Operation

CONTROL AND TIMING OF THE AD570/AD571

There are several important timing and control features on the AD570/AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 5.

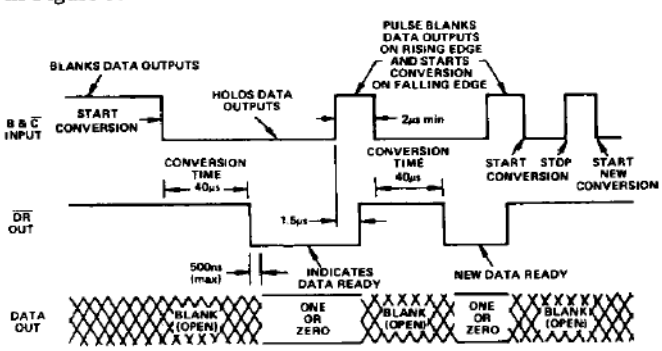


Figure 5. AD570/AD571 Timing and Control Sequences

The normal standby situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ will go high and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD570/AD571 discussed above allows the devices to be easily operated in a variety of systems with differing control modes. The two most common control modes, the convert pulse mode and the multiplex mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 6 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse.

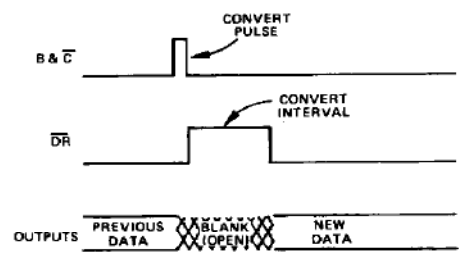


Figure 6. Convert Pulse Mode

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 7.

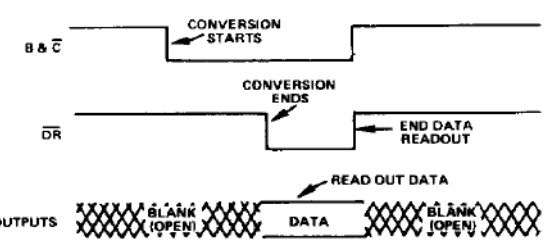


Figure 7. Multiplex Mode

This operating mode allows multiple converters to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several converters are multiplexed in sequence, a new conversion may be started in one AD570/AD571 while data is being read from another. As long as the data is read and the first AD570/AD571 is cleared within 15μs after the start of conversion of the second AD570/AD571, no data overlap will occur.