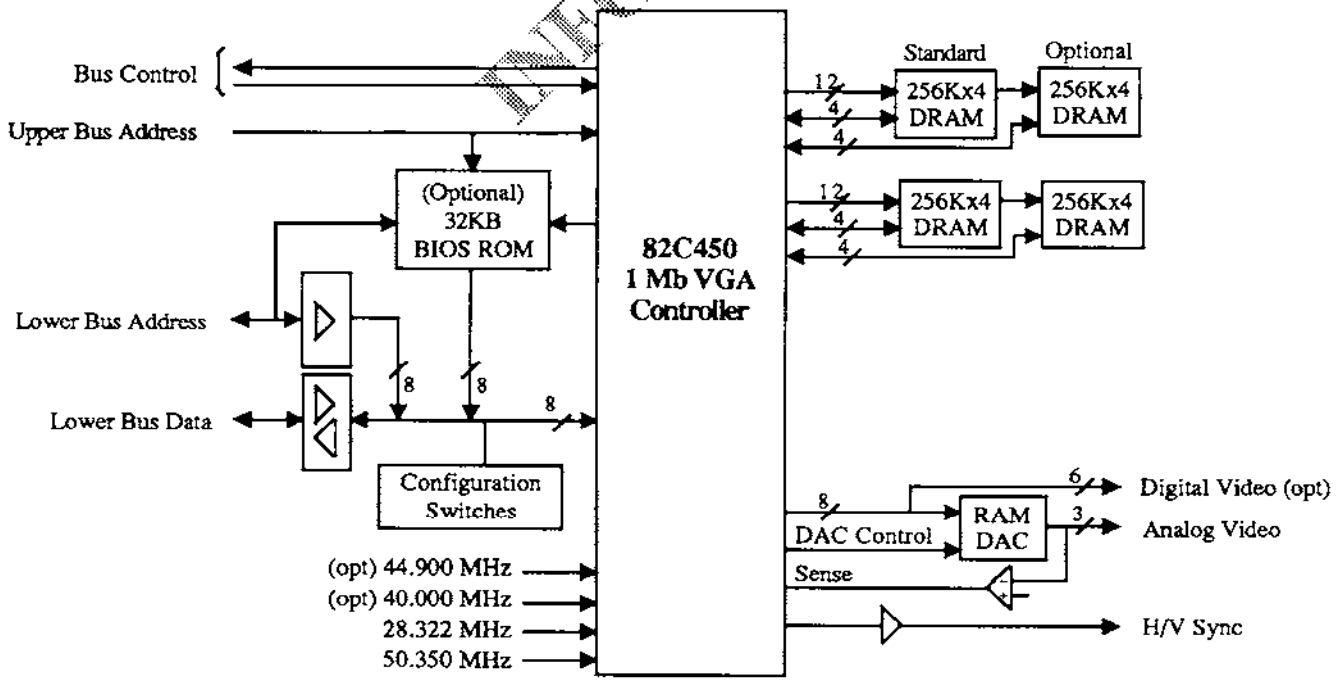
82C450
One Megabit DRAM VGA Graphics Controller

- Highly integrated design resulting in lower chip count. Total of 7 chips required for a VGA implementation including memory
- Supports two-chip and four-chip memory configurations using 256Kx4 DRAMs. Two DRAMs provide standard VGA modes. Four DRAMs provide extended modes and increased performance
- High performance resulting from zero wait-state writes (write buffer) and minimum wait-state reads (internal asynchronous FIFO design)
- Supports 16 color interlaced CRT displays to 1024x768 and Non-Interlaced to 800 x 600
- Fully Compatible with IBM™ VGA at hardware, register, and BIOS level
- Member of Chips & Technologies' ELEATSx CHIPSet
- Enhanced backward compatibility with EGA, CGA, Hercules™, and MDA without using NMIs
- Dual Bus Architecture, Integrated Interface to EISA/ISA (PC/AT) and MCA bus (CHIPS/250 and CHIPS/280)
- Supports use of frequency synthesis chips to minimize number of oscillators
- Single Chip Solution
- Small low-cost package: 100-pin flat pack
- Chip pinouts optimized for PCB layout
- Supports Digital and Analog Monitors
- External palette DAC support for up to 16 million colors
- Full complement of applications software drivers available from Chips and Technologies



82C450 System Diagram

Revision History

Revision	Date	By	Comment
0.75	7/31//90	ST	Internal Review
0.76	8/90	ST	Advanced Product Information Initial Release

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Introduction

VIDEO SUBSYSTEM CHIP COUNT

Using the 82C450, a complete VGA-compatible 8-bit video subsystem for motherboard applications can be built with just 7 ICs, including display memory, as shown in the following bill of materials table:

Qty	Chip type
1	82C450 VGA Chip
1	BT475 or BT477 RAMDAC
1	74LS245 Transceiver
1	74LS541 Buffer
1	74F04 Inverter
2	256Kx4 DRAMs
7	Total

Additional components required are 50.350 and 28.322 MHz oscillators, 15-pin video connector, and various resistors and capacitors. Support is also provided for frequency synthesis chips.

For add-in EISA/ISA-bus boards, an additional 27256 (32Kx8) BIOS ROM is required.

Support for 800x600x16-color graphics and 132-column text modes would require one additional 40 MHz oscillator (and four 256Kx4 DRAMs instead of two).

If Inmos RAMDACs or Brooktree 471/476 RAMDACs are used, then an additional LM339 comparator, LM334 current reference, and 1N4148 diode are required (the BT475 and BT477 RAMDACs shown in the bill of materials table in the column to the left incorporate the comparator and reference functions on-chip). The RAMDAC speed requirements should be compatible with the highest dotclock frequency used.

COMPATIBILITY

The 82C450 is a member of the CHIPS 45x VGA™ Controller product family. It is compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. It offers enhanced backward compatibility to EGA™, CGA™, Hercules™, and MDA™ standards on analog monitors without using NMIs.

The 82C450 provides on-chip support for EISA/ISA (PC/AT) and MCA (Microchannel) bus interfaces. Control signals for both types of interfaces are integrated on the chip, and support is also provided for 8-bit CPU interface for both memory and I/O cycles.

The 82C450 offers a lower cost system implementation by supporting operation with two or four 256Kx4 DRAMs.

DISPLAY MEMORY INTERFACE

The 82C450 supports two display memory configurations:

Two 256Kx4 DRAM devices (256Kbytes)
and
Four 256Kx4 DRAM devices (512Kbytes)

Implementing an 82C450 Video Subsystem with two 256Kx4 DRAMs results in a cost-efficient system by eliminating the need for eight 64Kx4 DRAMs. In this configuration the 82C450 supports all standard VGA display modes.

Performance is significantly improved when the 82C450 is configured with four 256Kx4 DRAMs. Standard VGA display modes are achieved along with 800x600 in 16 colors (non-interlaced planar graphics), 1024x768 in 16 colors (interlaced planar graphics) and 132-column text mode.

The entire display memory (256Kbytes or 512Kbytes) is always available to the CPU in regular four-plane mode, chained two-plane mode, and super-chained one-plane mode.

Display memory control signals are derived from the memory clock (MCLK) input.

CPU INTERFACE

The 82C450 has a strap option to select an EISA/ISA (PC/AT) Bus Interface or MCA (Microchannel) Bus Interface. All control signals for both interface types are integrated onto the single VGA chip.

Like the IBM VGA, the 82C450 supports 8-bit CPU interfaces only.

BIOS ROM INTERFACE

In EISA/ISA (PC/AT) Bus systems, the 82C450 supports an 8-bit BIOS with one external BIOS ROM chip. The ROM address is internally decoded and the transceivers are enabled directly by the 82C450. The 82C450 implements a ROM chip select (ROMCS/) pin to enable the ROM.

A 16-bit BIOS ROM could be implemented with the 82C450 using two BIOS ROM chips, an external PAL, and a 74LS244 buffer. However, a higher-

performance and lower-cost video system will result from implementation of an 8-bit BIOS ROM which is copied into system RAM by the system BIOS on startup.

For motherboard EISA/ISA-bus implementations, the video BIOS may alternately be incorporated directly into the system BIOS. In Microchannel-based systems, the video BIOS is always included in the system BIOS.

EXTENSION REGISTERS

All functionality of the extended registers in the 82C450 are disabled on reset. Before writing into the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). None of the unused bits in the regular VGA registers are used for extensions.

EXTERNAL COLOR PALETTE

The 82C450 supports the programming of an external color palette DAC (RAMDAC™) by decoding the CPU addresses and generating the READ and WRITE signals for the external palette.

Either Inmos™ or Brooktree™-style RAMDACs may be used. The 82C450 normally decodes 3C6-3C9 port addresses for the RAMDAC, but may be configured to additionally decode 83C6-83C9 port addresses for the Brooktree RAMDAC extension registers.

Normally, each RAMDAC analog output provides 6-bit resolution (64 shades of color on each of the analog R, G, and B outputs). If 8-bit-per-color mode is desired for the DAC (e.g., if using Inmos IMSG178 or Brooktree BT478 RAMDACs which provide 256 shades of color on each RGB output), the DAC's 6/8-bit mode pin must be controlled via logic external to the 82C450.

CONFIGURATION SWITCHES

The 82C450 can read up to eight configuration bits. These signals are sampled on data bus bits AD0-AD7 on the falling edge of RESET. The state of AD0 on RESET determines EISA/ISA bus (default) or MCA bus interface and AD1 determines whether ROM decode is enabled in ISA bus systems. AD2 determines the pixel clock source and AD3 determines whether memory timing comes from 50.350 MHz. AD4-7 are currently reserved for future use. All eight bits are latched into an extension register on RESET so software may determine the hardware configuration. Also, the reserved bits may optionally be used to read external switches or status bits (such as the monitor sense bits MS0-2 from the Analog Video connector).

Selected AD lines should be externally connected to 10K pulldown resistors (or driven low while RESET is high) in order to be sampled on the falling edge of RESET as low inputs. The 82C450 implements internal high-value pullup resistors on all AD pins, so that other AD pins could theoretically be left unconnected. However, it is recommended to connect the other AD lines to 10K pullup resistors or drive them high with a 3-state buffer during RESET.

VIRTUAL SWITCH REGISTER

The 82C450 implements a 'virtual switch register'. In 'EGA' mode, the sense bit of the Feature control register (3C2 bit 4) may be set up to read a selected bit from the 'virtual switch register' (an extension register set up by BIOS at initialization time) instead of reading the state of the SENSE pin. This reduces overall video subsystem chip count by eliminating the external multiplexers otherwise required on the sense pin.

CLOCK SELECTION

The 82C450 provides separate inputs for dot clock selections 0, 1, 2, and 3 (called CLK0, CLK1, CLK2, and CLK3) which are normally selected by Misc Output Register bits 2 and 3. By default, CLK0 and CLK1 are inputs which must be connected to 50.350 MHz and 28.322 MHz for implementation of standard VGA capabilities. The CLK0 input provides the memory clock (the CLK0 input is internally divided by two in the 82C450 for the required 25.175 MHz dotclock). Alternately a 56.644 MHz memory clock can be provided on the CLK1 pin, with 50.35 MHz on CLK0 (both are internally divided by two). 50.35 MHz memory clock is used with 120ns DRAMs. 56.644 MHz memory clock is used with 100ns DRAMs. If desired, extended capabilities may be implemented, such as 800x600 sixteen-color graphics mode and 132-column text mode, by connecting a 40.000 MHz oscillator to CLK2. Interlaced 1024x768 sixteen-color mode can be implemented by connecting 44.9 MHz to the CLK3 input. The 82C450 internally selects between these inputs so no additional circuitry is required.

Alternately, the CLK2 and CLK3 pins may be selected as outputs to provide Misc Output Register bits 2 and 3 externally to the chip. This allows clock selection to be implemented externally with the dot clock input always on CLK1 and fixed 50.350 or 56.644 MHz memory clock on CLK0. This allows

an external clock synthesizer chip to be used and provides one additional user-defined frequency to be selected.

PACKAGE

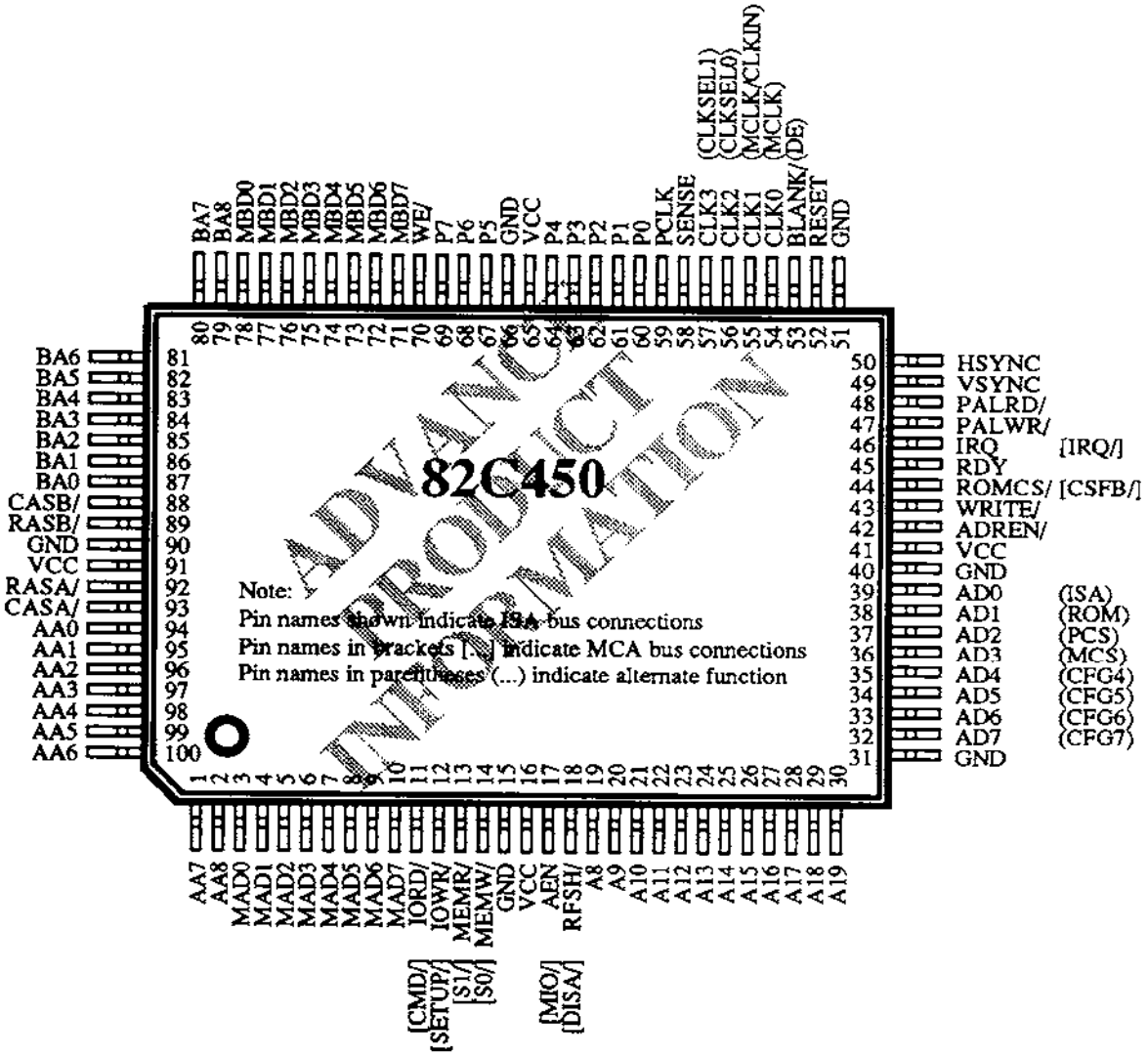
The 82C450 is available in a 100-pin plastic flat pack (PFP). Complete descriptions of all 82C450 pins are included in this document. The pins are separated into the following logical groups for discussion: Bus Interface, Display Memory, Video, Clock, Power, and Ground.

APPLICATION SCHEMATIC EXAMPLES

Included in this document are application schematic examples of the following:

1. 8-bit EISA/ISA Bus Interface
   8-bit MCA Bus Interface
2. Memory Interfacing (2 or 4 256Kx4 DRAMs)
3. Video Interface (Inmos RAMDAC)
   Video Interface (Brooktree RAMDAC)
4. Clock Interface - Minimum Configurations
   Clock Interface - Alternate Configurations

82C450 Pinouts



82C450 PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name		Type	Active	Description
30	A19		In	High	System Upper Address Bus
29	A18		In	High	
28	A17		In	High	
27	A16		In	High	
26	A15		In	High	
25	A14		In	High	
24	A13		In	High	
23	A12		In	High	
22	A11		In	High	
21	A10		In	High	
20	A9		In	High	
19	A8		In	High	
32	AD7	(CFG7)	I/O	High	System Address/Data Bus and Configuration Inputs. AD0-7 are sampled on the falling edge of RESET and latched into XR01. ISA determines whether the bus interface is EISA/ISA (1) or MCA (0). ROM high enables decode of the BIOS ROM address space (C0000-C7FFF). PCS (Pixel Clock Source) determines whether CLK2-3 are inputs (1) or outputs for a clock generator chip (0). MCS (Memory Clock Source) determines whether memory timing comes from CLK0 (1) or CLK1 (0). AD4-7 have no hardware function.
33	AD6	(CFG6)	I/O	High	
34	AD5	(CFG5)	I/O	High	
35	AD4	(CFG4)	I/O	High	
36	AD3	(MCS)	I/O	High	
37	AD2	(PCS)	I/O	High	
38	AD1	(ROM)	I/O	High	
39	AD0	(ISA)	I/O	High	
42	ADREN/		Out	Low	Address buffer enable (forced low during RESET)
43	WRITE/		Out	Low	Data transceiver direction (forced high during RESET)
44	ROMCS/	[CSFB/]	Out	Low	ROM Chip Select (EISA/ISA bus) or Card Select Feedback (MCA bus).
45	RDY		Out	High	Ready. Driven low to indicate that current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then 3-stated.
46	IRQ	[IRQ/]	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. (EISA/ISA-Bus interrupts are active high, MCA bus interrupts are active low). See also XR14 bit–7.
52	RESET		In	High	Reset. Connect directly to the bus reset signal.

ADREN/	WRITE/	Function
0	0	Normal (address input) state
0	1	Reset (AD bus undriven)
1	0	Data write to VGA chip
1	1	Data read from VGA chip

Note: Pin names in brackets [...] indicate MCA bus functionality if different from EISA/ISA (PC/AT) bus

82C450 PIN DESCRIPTIONS — System Bus Interface (continued)

Pin #	Pin Name		Type	Active	Description
17	AEN	[MIO/]	In	Both	In EISA/ISA interface, defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally). In MCA interface, indicates memory or I/O cycle: 1 = memory, 0 = I/O.
18	RFSH/	[DISA/]	In	Low	This pin is an active low signal indicating Refresh cycle. When this pin is low, the memory is not accessible.
11	IORD/	[CMD/]	In	Low	In EISA/ISA interface, indicates I/O Read Cycle. In MCA interface, indicates beginning of a command part of a bus cycle. Driven off CMD/ on MCA, VGACMD/ on CHIPS/250.
12	IOWR/	[SETUP/]	In	Low	In EISA/ISA interface, indicates I/O Write Cycle. In MCA interface, indicates that the configuration register at 100-107 should be enabled. All other memory and I/O functions are disabled.
13	MEMR/	[S1/]	In	Low	In EISA/ISA interface, indicates Memory Read cycle. In MCA interface, indicates Status 1.
14	MEMW/	[S0/]	In	Low	In EISA/ISA interface, indicates Memory Write cycle. In MCA interface, indicates Status 0. S1/ S0/ Operation 0 0 Undefined 0 1 Read 1 0 Write 1 1 Undefined
48	PALRD/		Out	Low	Connected to the Read input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C450 is enabled and an I/O Read occurs from addresses 3C6h, 3C8h, or 3C9h. (The 82C450 responds directly for accesses to 3C7h).
47	PALWR/		Out	Low	Connected to the Write input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C450 is enabled and an I/O Write occurs to addresses 3C6-3C9h.

Note: Pin names in brackets [...] indicate MCA bus functionality if different from EISA/ISA (PC/AT) bus

82C450 PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name	Type	Active	Description
2	AA8	Out	High	DRAM address bus for planes 0-1
1	AA7	Out	High	
100	AA6	Out	High	
99	AA5	Out	High	
98	AA4	Out	High	
97	AA3	Out	High	
96	AA2	Out	High	
95	AA1	Out	High	
94	AA0	Out	High	
79	BA8	Out	High	DRAM address bus for planes 2-3
80	BA7	Out	High	
81	BA6	Out	High	
82	BA5	Out	High	
83	BA4	Out	High	
84	BA3	Out	High	
85	BA2	Out	High	
86	BA1	Out	High	
87	BA0	Out	High	
10	MAD7	I/O	High	DRAM data bus for planes 0-1 (MAD4-7 are not connected in 2-DRAM configurations)
9	MAD6	I/O	High	
8	MAD5	I/O	High	
7	MAD4	I/O	High	
6	MAD3	I/O	High	
5	MAD2	I/O	High	
4	MAD1	I/O	High	
3	MAD0	I/O	High	
71	MBD7	I/O	High	DRAM data bus for planes 2-3 (MBD4-7 are not connected in 2-DRAM configurations)
72	MBD6	I/O	High	
73	MBD5	I/O	High	
74	MBD4	I/O	High	
75	MBD3	I/O	High	
76	MBD2	I/O	High	
77	MBD1	I/O	High	
78	MBD0	I/O	High	
70	WE/	Out	Low	Write enable for all memory banks/planes
92	RASA/	Out	Low	Row address strobe for memory planes 0-1
89	RASB/	Out	Low	Row address strobe for memory planes 2-3
93	CASA/	Out	Low	Column address strobe for memory planes 0-1
88	CASB/	Out	Low	Column address strobe for memory planes 2-3

82C450 PIN DESCRIPTIONS

Video Interface

Pin #	Pin Name		Type	Active	Description
69	P7		Out	High	8-bit video output
68	P6		Out	High	
67	P5		Out	High	
64	P4		Out	High	
63	P3		Out	High	
62	P2		Out	High	
61	P1		Out	High	
60	P0		Out	High	
59	PCLK		Out	High	Video Pixel Clock. Video data is synchronized to this clock.
50	HSYNC		Out	Both	Horizontal sync for CRT (polarity is programmable)
49	VSYNC		Out	Both	Vertical sync for CRT (polarity is programmable)
53	BLANK/	(DE)	Out	Both	Blanking signal for external palette DAC (polarity is programmable; see XR28 bit-0). May also be redefined as Display Enable (see XR28 bit-1).
58	SENSE		In	High	Input pin normally used for reading monitor sense. Normally connected to the outputs of an LM339 comparator on the analog RGB outputs. The state of this pin may read as bit-4 of Input Status Register 0 (port 3C2h). See also extension register XR1F (Virtual Switch Register).

82C450 PIN DESCRIPTIONS

Clock, Power, and Ground

Pin #	Pin Name		Type	Active	Description
54	CLK0	(MCLK)	In	High	If internal clock selection is enabled (default), CLK0, CLK1, CLK2, and CLK3 are inputs. One of the four is selected as the input dotclock per Misc Output Register (3C2h) bits 2 and 3. Memory clock may be selected from either CLK0 or CLK1 (see pin AD3 and configuration register XR01); if CLK0 is selected as MCLK, 50.35 MHz is used (CLK1 is 28.322); if CLK1 is selected as MCLK, 56.644 MHz is used (CLK0 is 25.175). If external clock selection is enabled (see pin AD2 and configuration register XR01), CLKIN becomes the input dotclock for all pixel clock frequencies and CLK2-3 become clock select outputs driven by Misc Output Register (3C2h) bits 2 and 3. In this mode, the CLK0 pin is always used for memory timing (MCLK).
55	CLK1	(MCLK/CLKIN)	In	High	
56	CLK2	(CLKSEL0)	I/O	High	
57	CLK3	(CLKSEL1)	I/O	High	
16	VCC		VCC	--	Power
41	VCC		VCC	--	
65	VCC		VCC	--	
91	VCC		VCC	--	
15	GND		GND	--	Ground
31	GND		GND	--	
40	GND		GND	--	
51	GND		GND	--	
66	GND		GND	--	
90	GND		GND	--	

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82C450 REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
STAT	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
CONFIG	Hercules Configuration	2	W	3BF	n/a	
			R	3B6-3B7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C450 REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MISC	Miscellaneous Output	7	W	3C2	3C2	
FC	Feature Control	3	W	3BA	3DA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	
STAT	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3BC (ignored)	3DC (ignored)	ref only: no light pen
SRX, SR0-4	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-18	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-13	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

82C450 REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Reg Type	Comment
POSIDL	POS ID LSB	8	R	100 (Setup Only)	100 (Setup Only)	Motherboard	ref only
POSIDH	POS ID MSB	8	R	101 (Setup Only)	101 (Setup Only)	Motherboard	ref only
SLEEP	Video Subsystem Sleep Control	1	RW	102 (Setup Only)	102 (Setup Only)	VGA	full decode
XENA	Extended Enable	7	RW	103 (Setup Only)	103 (Setup Only)	VGA	full decode
GLOBID	Global ID (0A5h)	8	R	104 (Setup Only)	104 (Setup Only)	VGA	full decode
MISC	Miscellaneous Output	7	W	3C2	3C2	VGA	
			R	3CC	3CC	VGA	
FC	Feature Control	3	W	3BA	3DA	VGA	
			R	3CA	3CA	VGA	
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2	VGA	
STAT	Display Status (Input Status 1)	6	R	3BA	3DA	VGA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	n/a	no lpen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3BC (ignored)	3DC (ignored)	n/a	no lpen
VSE	Video Subsystem Enable	1	RW	3C3 if MCA	3C3 if MCA	Motherboard	
46E8	Setup / Disable Control	2	W	46E8 if ISA	46E8 if ISA	VGA	
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	DAC	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	VGA	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	DAC	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	DAC	
DACDATA	Color Palette Registers 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	DAC	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	VGA	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	VGA	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	VGA	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	VGA	
XRX, XR0-7F	Extension Registers	0-8	RW	3B6-3B7	3D6-3D7	VGA	103 bit7=1

82C450 REGISTER SUMMARY - INDEXED REGISTERS (EGA / VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

82C450 EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' 45x Product Family 450	451	452	453	455	456
XRX	Extension Index Register	7	R/W	3B6/3D6	0xxxxxxx	✓	✓	✓	x	✓	✓
XR00	Chip Version	8	R/O	3B7/3D7	0100rrrr	✓	✓	✓	x	✓	✓
XR01	DIP Switch	8	R/O	3B7/3D7	dddddddd	✓	✓	✓	x	✓	✓
XR02	CPU Interface	8	R/W	3B7/3D7	RRRRRRRR	✓	✓	✓	x	✓	✓
XR03	*(ROM Interface)*	–	–	3B7/3D7		.	✓	✓	x	.	.
XR04	Memory Mapping	2	R/W	3B7/3D7	00R0000R	✓	✓	✓	.	✓	✓
XR05	*(Sequencer Control)*	–	–	3B7/3D7		.	.	✓	x	.	.
XR06	*(DRAM Interface)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR07	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.
XR08	*(General Purpose Output Select B)*	–	–	3B7/3D7		.	✓	✓	.	✓	✓
XR09	*(General Purpose Output Select A)*	–	–	3B7/3D7		.	✓	✓	.	✓	✓
XR0A	*(Cursor Address Top)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR0B	CPU Paging	3	R/W	3B7/3D7	00000RRR	✓	.	✓	x	✓	✓
XR0C	Start Address Top	1	R/W	3B7/3D7	0000000R	✓	.	✓	x	.	.
XR0D	Auxiliary Offset	2	R/W	3B7/3D7	000000RR	✓	✓	✓	x	✓	✓
XR0E	Text Mode	2	R/W	3B7/3D7	0000RR00	✓	.	✓	.	.	.
XR0F	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.
XR10	Single/Low Map Register	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	x	.	.
XR11	High Map Register	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	x	.	.
XR12	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.
XR13	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.
XR14	Emulation Mode	8	R/W	3B7/3D7	RRRRhhRR	✓	✓	✓	x	✓	✓
XR15	Write Protect	7	R/W	3B7/3D7	RRRRRRRR	✓	✓	✓	x	✓	✓
XR16	*(Trap Enable)*	–	–	3B7/3D7		.	✓	✓	x	✓	✓
XR17	*(Trap Status)*	–	–	3B7/3D7		.	✓	✓	x	✓	✓
XR18	Alternate H Display End	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR19	Alt H Retr Start/Half-line Comp	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR1A	Alternate H Retrace End	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR1B	Alternate H Total	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR1C	Alternate H Blank Start	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR1D	Alternate H Blank End	8	R/W	3B7/3D7	Rxxxxxxx	✓	✓	✓	x	✓	✓
XR1E	Alternate Offset	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	x	✓	✓
XR1F	Virtual EGA Switch Register	4	R/W	3B7/3D7	0000xxxx	✓	.	.	x	.	.
XR20	*(Sliding Unit Delay)/(453 Interface)*	–	–	3B7/3D7		.	.	✓	x	.	.
XR21	*(Sliding Hold A)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR22	*(Sliding Hold B)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR23	*(Sliding Hold C)/(Wr Bit Mask Ctrl)*	–	–	3B7/3D7		.	.	✓	x	.	.
XR24	*(Sliding Hold D)/(Wr Bit Mask Pattern)*	–	–	3B7/3D7		.	.	✓	x	.	.
XR25	*(453 Pin Definition)*	–	–	3B7/3D7		.	.	.	x	.	.
XR26	*(453 Configuration)*	–	–	3B7/3D7		.	.	.	x	.	.
XR27	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.
XR28	Video Interface	4	R/W	3B7/3D7	00R00RRR	✓	✓	✓	x	✓	✓
XR29	*(Function Control)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR2A	*(Frame Interrupt Count)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR2B	Default Video	8	R/W	3B7/3D7	RRRRRRRR	✓	✓	✓	.	✓	✓
XR2C	*(Force Horizontal High)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR2D	*(Force Horizontal Low)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR2E	*(Force Vertical High)*	–	–	3B7/3D7		.	.	✓	.	.	.
XR2F	*(Force Vertical Low)*	–	–	3B7/3D7		.	.	✓	.	.	.

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
0 = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
R = Reset to 0 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 451 = Integrated VGA, 452 = Super VGA, 455 & 456 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

82C450 EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' 45x Product Family 450	451	452	455	456
XR30	*(Graphics Cursor Start Address High)*	–	–	3B7/3D7		.	.	✓	.	.
XR31	*(Graphics Cursor Start Address Low)*	–	–	3B7/3D7		.	.	✓	.	.
XR32	*(Graphics Cursor End Address)*	–	–	3B7/3D7		.	.	✓	.	.
XR33	*(Graphics Cursor X Position High)*	–	–	3B7/3D7		.	.	✓	.	.
XR34	*(Graphics Cursor X Position Low)*	–	–	3B7/3D7		.	.	✓	.	.
XR35	*(Graphics Cursor Y Position High)*	–	–	3B7/3D7		.	.	✓	.	.
XR36	*(Graphics Cursor Y Position Low)*	–	–	3B7/3D7		.	.	✓	.	.
XR37	*(Graphics Cursor Mode)*	–	–	3B7/3D7		.	.	✓	.	.
XR38	*(Graphics Cursor Mask)*	–	–	3B7/3D7		.	.	✓	.	.
XR39	*(Graphics Cursor Color 0)*	–	–	3B7/3D7		.	.	✓	.	.
XR3A	*(Graphics Cursor Color 1)*	–	–	3B7/3D7		.	.	✓	.	.
XR3B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR3F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR40	*(I/O Flag)*	–	–	3B7/3D7		.	.	.	.	.
XR41	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR42	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR43	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR44	*(Scratch Register 0)*	–	–	3B7/3D7		.	.	.	.	.
XR45	*(Scratch Register 1 / FG Color)*	–	–	3B7/3D7		.	.	.	.	.
XR46	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR47	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR48	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR49	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4A	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR4F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR50	*(Panel Format)*	–	–	3B7/3D7		.	.	.	✓	✓
XR51	*(Display Type)*	–	–	3B7/3D7		.	.	.	✓	✓
XR52	*(Panel Size)*	–	–	3B7/3D7		.	.	.	✓	✓
XR53	*(Override)*	–	–	3B7/3D7		.	.	.	✓	✓
XR54	*(Alternate Misc Output)*	–	–	3B7/3D7		.	.	.	✓	✓
XR55	*(Text Mode 350_A Compensation)*	–	–	3B7/3D7		.	.	.	✓	✓
XR56	*(Text Mode 350_B Compensation)*	–	–	3B7/3D7		.	.	.	✓	✓
XR57	*(Text Mode 400 Compensation)*	–	–	3B7/3D7		.	.	.	✓	✓
XR58	*(Graphics Mode 350 Compensation)*	–	–	3B7/3D7		.	.	.	✓	✓
XR59	*(Graphics Mode 400 Compensation)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5A	*(Flat Panel Vertical Display Start 400)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5B	*(Flat Panel Vertical Display End 400)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5C	*(Weight Control Clock A)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5D	*(Weight Control Clock B)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5E	*(ACDCLK Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR5F	*(Power Down Mode Refresh)*	–	–	3B7/3D7		.	.	.	✓	✓

82C450 EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' 45x Product Family 450	451	452	455	456
XR60	*(Blink Rate Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR61	*(Text Color Mapping Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR62	*(Text Color Shift Parameter)*	–	–	3B7/3D7		.	.	.	✓	✓
XR63	*(Graphics Color Mapping Control)*	–	–	3B7/3D7		.	.	.	✓	✓
XR64	*(Alternate Vertical Total)*	–	–	3B7/3D7		.	.	.	✓	✓
XR65	*(Alternate Overflow)*	–	–	3B7/3D7		.	.	.	✓	✓
XR66	*(Alternate Vertical Sync Start)*	–	–	3B7/3D7		.	.	.	✓	✓
XR67	*(Alternate Vertical Sync End)*	–	–	3B7/3D7		.	.	.	✓	✓
XR68	*(Alternate Vertical Display Enable End)*	–	–	3B7/3D7		.	.	.	✓	✓
XR69	*(Flat Panel Vertical Display Start 350)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6A	*(Flat Panel Vertical Display End 350)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6B	*(Flat Panel Vertical Overflow 2)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6C	*(Weight Control Clock C)*	–	–	3B7/3D7		.	.	.	✓	✓
XR6D	*(External Palette Control)*	–	–	3B7/3D7		.	.	.	.	✓
XR6E	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR6F	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR70	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR71	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR72	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR73	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR74	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR75	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR76	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR77	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR78	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR79	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7A	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7B	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7C	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7D	-reserved-	–	–	3B7/3D7		.	.	.	.	.
XR7E	**CGA/Hercules Color Select**	6	R/O	3B7/3D7	00xxxxxx	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	7	R/W	3B7/3D7	RRxxxxRR	✓	✓	✓	✓	✓

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82C450 Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode. This register is used only in the PC-bus interface. In the MCA Bus interface these functions are performed by the DISA/ and SETUP/ pins respectively.

The Global and Extension Enable Registers are accessible only during Setup mode. The Global ID Register contains the ID number that identifies the 82C450 as a Chips & Technologies product.

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space*. Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 82C450 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/HSYNC output, and vertical retrace/video output. The Feature Control Register selects the VSYNC function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video SYNC polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32KBytes, Odd/Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to the 82C450 in the external color palette. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 82C450 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address (3Bx/3Dxh) and Read/Write access to the extension registers are controlled by the Extension Enable Register (103h).

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

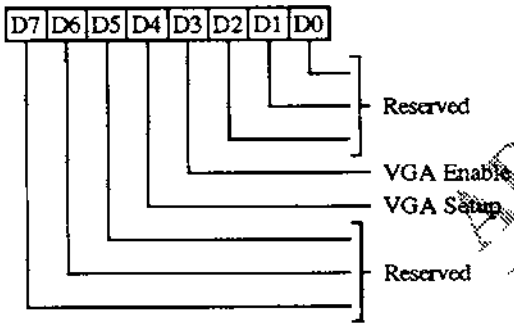
1. Miscellaneous Registers include the 82C450 Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.

Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 82C450 (Extension Registers) are summarized in the Extension Register Table.

82C450 Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Setup Control	–	W	46E8h (PC-Bus only)	–	23
–	Global Enable	–	RW	102h & Setup mode	–	23
–	Extension Enable	–	RW	103h & Setup mode	–	24
–	Global ID	–	R	104h & Setup mode	–	24

SETUP CONTROL REGISTER
Write only at I/O Address 46E8h



This register is used with the PC-Bus Interface only. It is cleared by RESET. In the MCA interface, the Setup mode and VGA Disable are controlled through the SETUP/ and DISA/ pins, respectively.

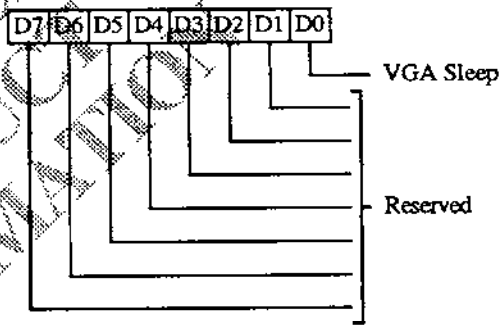
2-0 Reserved (0)

3 VGA Enable
- 0: VGA is disabled
- 1: VGA is enabled

4 Setup Mode
- 0: VGA is in Normal Mode
- 1: VGA is in Setup Mode

7-5 Reserved (0)

GLOBAL ENABLE REGISTER
Read/Write at I/O Address 102h

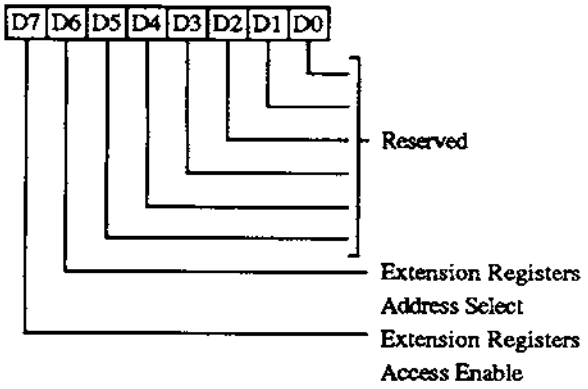


This register is only accessible in Setup Mode. It is cleared by RESET.

0 VGA Sleep
- 0: VGA is disabled
- 1: VGA is enabled

7-1 Reserved (0)

EXTENSION ENABLE REGISTER
Read/Write at I/O Address 103h



This register is only accessible in Setup Mode. It is cleared by RESET.

3-0 Reserved (0)

4 Reserved (0) This bit must be set to zero for proper operation of the 82C450.

5 Reserved (0)

6 Address for Extension Registers

0: Extension registers at I/O Address 3D6/3D7h

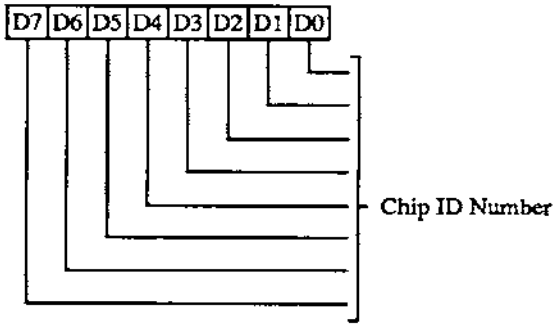
1: Extension registers at I/O Address 3B6/3B7h.

7 Extension Registers Access Enable

This bit controls access to the extension registers at 3D6/7 or 3B6/7. It also allows access to all CGA, MDA and Hercules registers in non-emulation mode.

0: Disable Access
1: Enable Access

GLOBAL ID REGISTER
Read only at I/O Address 104h



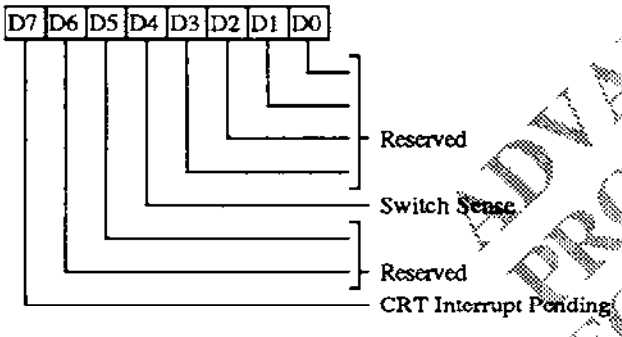
This register is only accessible in Setup Mode.

7-0 These bits contain the ID number (0A5h). This identifies the chip as a Chips and Technologies product.

82C450 General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	25
ST01	Input Status 1	–	R	3BAh/3DAh	–	25
FCR	Feature Control	–	W	3BAh/3DAh	5	26
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	26
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h



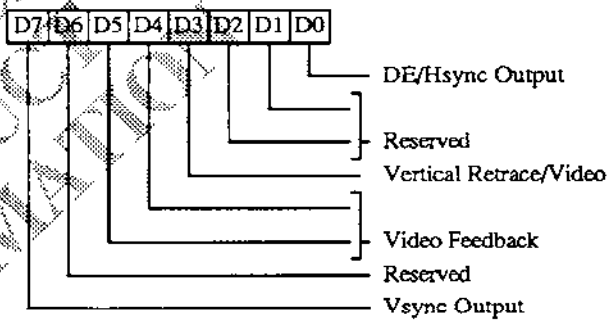
3-0 Reserved (0)

4 Switch Sense. This bit returns the Status of the SENSE pin.

6-5 Reserved. These bits read back 00 in an AT bus implementation and 11 in MCA implementation.

7 CRT Interrupt Pending
- 0: Indicates no CRT interrupt is pending
- 1: Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output. The functionality of this bit is controlled by the Emulation Mode register (XR14[4]).
- 0: Indicates DE or HSYNC inactive
- 1: Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video. The functionality of this bit is controlled by the Emulation Mode register (XR14[5]).
- 0: Indicates VSYNC or video inactive
- 1: Indicates VSYNC or video active

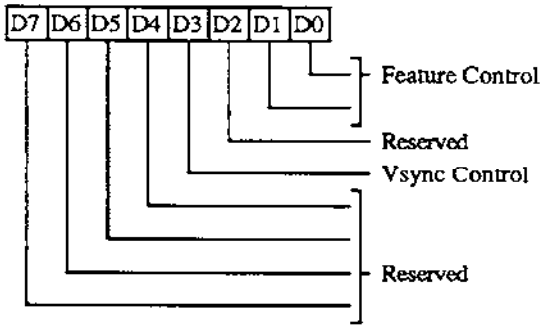
5-4 Video Feedback 1, 0. These are diagnostic video bits which are selected via the Color Plane Enable Register.

6 Reserved (0)

7 Vsync Output. The functionality of this bit is controlled by the Emulation Mode register (XR14[6]). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control. These bits are used internal to the 82C450 in conjunction with the Configuration Register (XR01). When enabled by XR01 bits 2-3 and Misc Output Register bits 3-2 = 10, these bits determine the pixel clock frequency typically as follows:

FCR1:0 = 00 = 40.000 MHz
FCR1:0 = 01 = 50.350 MHz
FCR1:0 = 10 = User defined
FCR1:0 = 11 = 44.900 MHz

This preserves compatibility with drivers developed for the 82C451 and 82C452 VGA controllers.

2 Reserved (0)

3 Vsync Control This bit is cleared by RESET.

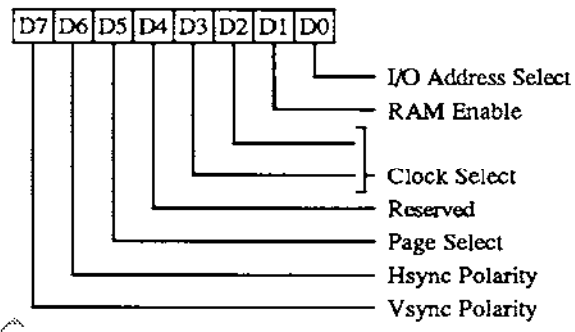
0: VSync output on the VSYNC pin
1: Logical 'OR' of VSync and Display Enable output on the VSYNC pin

This capability is not typically very useful, but is provided for IBM compatibility.

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0: Select 3Bxh I/O address
1: Select 3Dxh I/O address

1 Enable RAM. 0: Prevent CPU access to display memory; 1: Allow CPU access to display memory.

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.

6 CRT Hsync Polarity. 0=pos, 1=neg
7 CRT Vsync Polarity. 0=pos, 1=neg

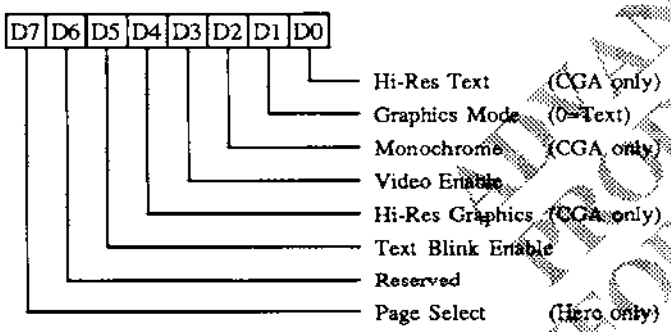
(Blank pin polarity can be controlled via the Video Interface Register, XR28)

82C450 CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	27
COLOR	CGA Color Select	–	RW	3D9h	–	28
HCFG	Hercules Configuration	–	RW	3BFh	–	29

CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
- 0: Select 40 column CGA text mode
- 1: Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
- 0: Select text mode
- 1: Select graphics mode

2 CGA Mono/Color Mode
- 0: Select CGA color mode
- 1: Select CGA monochrome mode

3 CGA/Hercules Video Enable
- 0: Blank the screen
- 1: Enable video output

4 CGA High Resolution Mode
- 0: Select 320x200 graphics mode
- 1: Select 640x200 graphics mode

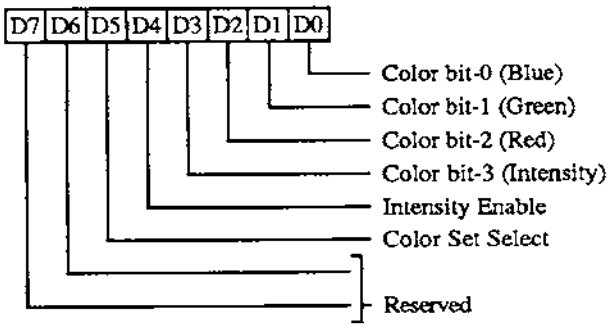
5 CGA/Hercules Text Blink Enable
- 0: Disable character blink attribute (blink attribute bit-7 used to control background intensity)
- 1: Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
- 0: Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
- 1: Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

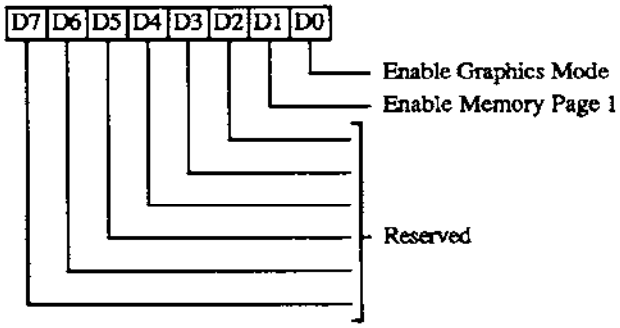
5 Color Set Select. This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)

Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by RESET.

0 Enable Graphics Mode

- 0: Lock the 82C450 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).
- 1: Permit entry to Hercules Graphics mode.

1 Enable Memory Page 1

- 0: Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.
- 1: The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

7-2 Reserved (0)

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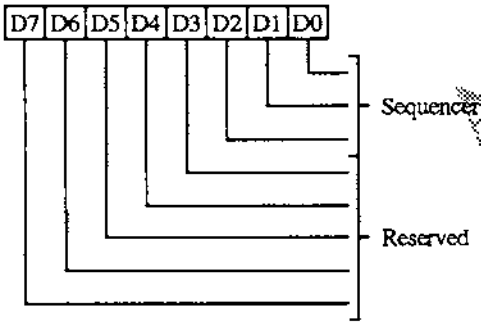
82C450 Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	31
SR00	Reset	00h	RW	3C5h	1	31
SR01	Clocking Mode	01h	RW	3C5h	1	32
SR02	Plane/Map Mask	02h	RW	3C5h	1	32
SR03	Character Font	03h	RW	3C5h	1	33
SR04	Memory Mode	04h	RW	3C5h	1	34
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	34

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



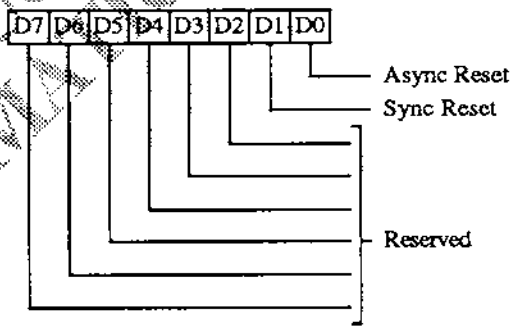
This register is cleared by RESET.

2-0 These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0: Force asynchronous reset
1: Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

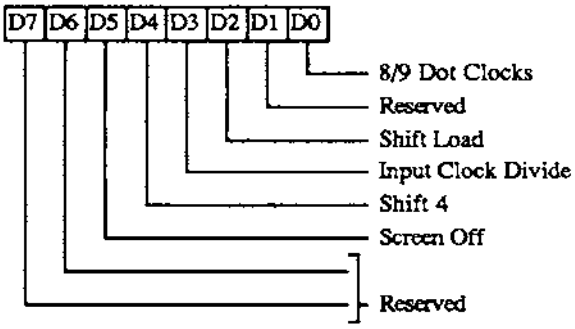
0: Force synchronous reset
1: Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks. This bit determines whether a character clock is 8 or 9 dot clocks long.
- 0: Select 9 dots/character clock
- 1: Select 8 dots/character clock

1 Reserved (0)

2 Shift Load
- 0: Load video data shift registers every character clock
- 1: Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide
- 0: Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
- 1: Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

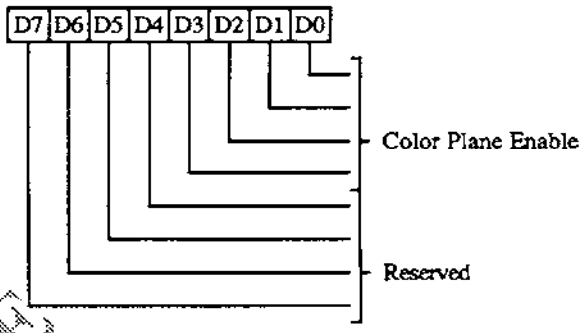
4 Shift 4
- 0: Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
- 1: Load shift registers every 4th character clock.

5 Screen Off
- 0: Normal Operation
- 1: Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection

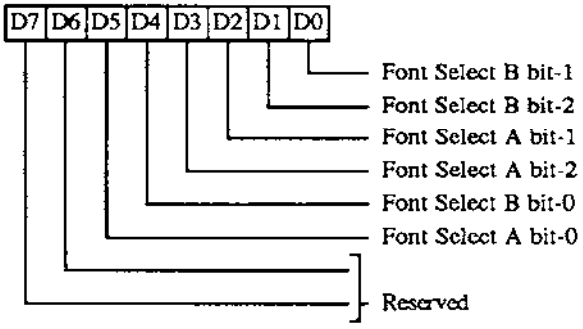


3-0 Color Plane Enable
- 0: Write protect corresponding color plane
- 1: Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

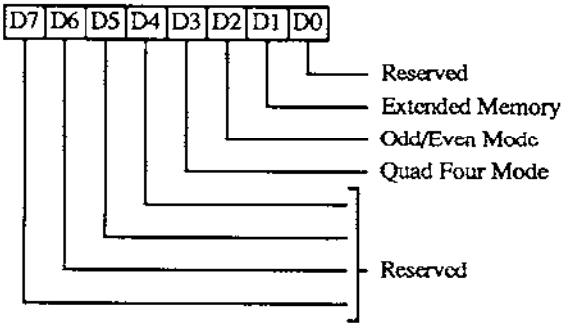
where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)

Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

0: Restrict CPU access to 4/16/32 Kbytes
1: Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

3 Quad Four Mode

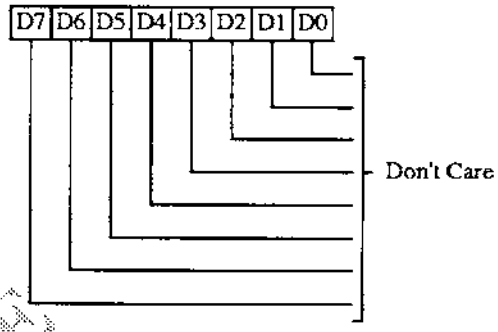
0: CPU addresses are mapped to display memory as defined by bit-2 of this register
1: CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)

Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

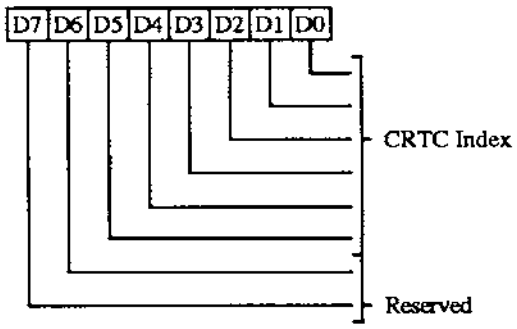
82C450 CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	36
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	36
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	36
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	37
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	37
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	38
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	38
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	39
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	39
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	40
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	40
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	41
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	41
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	42
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	42
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	42
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	42
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	43
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	43
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	43
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	43
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	44
CR13	Offset	13h	RW	3B5h/3D5h	3	44
CR14	Underline Row	14h	RW	3B5h/3D5h	3	44
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	45
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	45
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	46
CR18	Line Compare	18h	RW	3B5h/3D5h	3	47
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	48
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	48
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	48

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 D7) of whether the vertical sync or light pen registers are readable at indices 10-11.

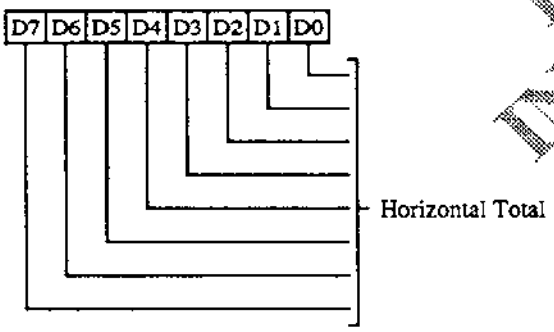
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC data register index

7-6 Reserved (0)

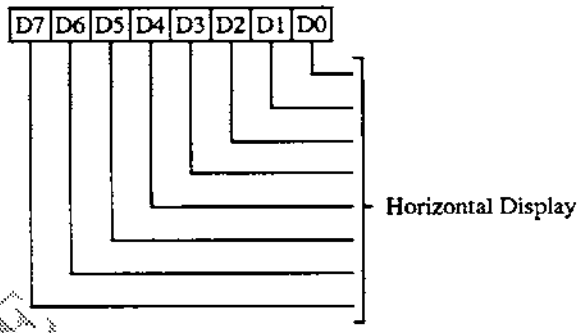
HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 protection

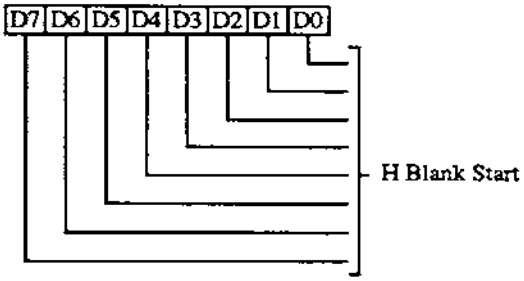


This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)

Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 protection

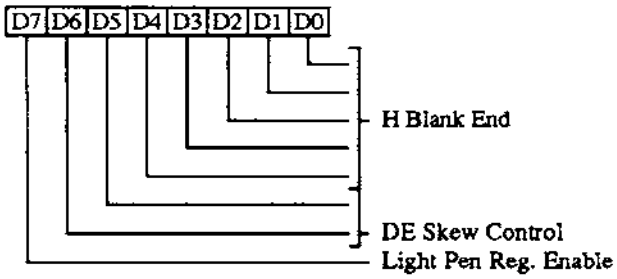


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)

Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

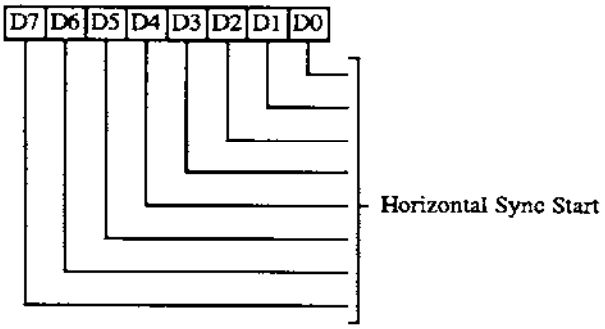
4-0 These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 D7. This bit = [(CR02 + W) and 20h]/20h.

6-5 Display Enable Skew Control: Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Reg. Enable: Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 protection

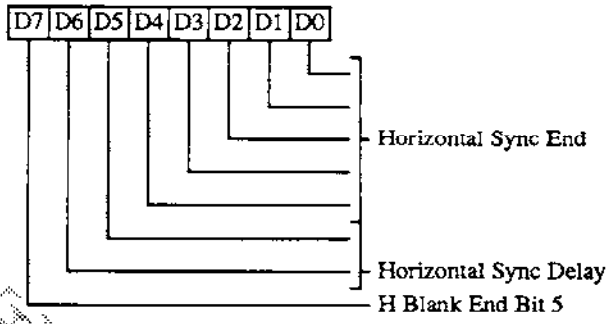


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

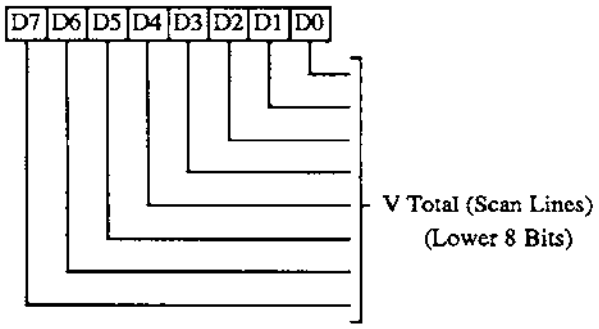
4-0 Hsync End. Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay. These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5. Sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 protection



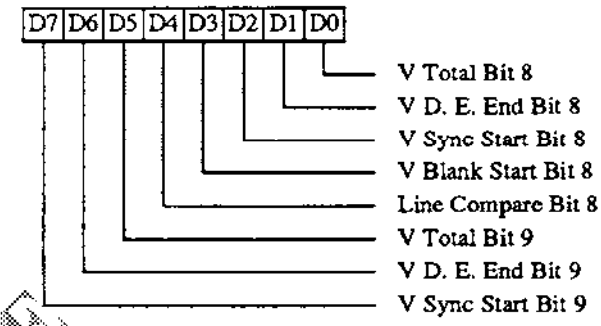
This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 protection on bits 0-3 and bits 5-7
Group 3 protection on bit 4

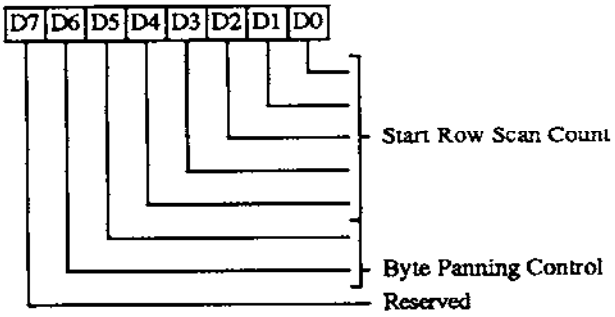


This register is used in all modes.

0	Vertical Total Bit 8
1	Vertical Display Enable End Bit 8
2	Vertical Sync Start Bit 8
3	Vertical Blank Start Bit 8
4	Line Compare Bit 8
5	Vertical Total Bit 9
6	Vertical Display Enable End Bit 9
7	Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



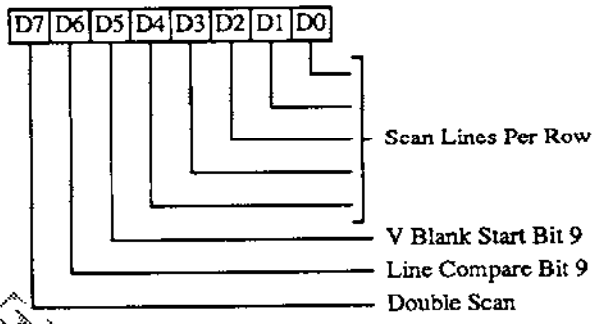
4-0 These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control. These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 protection on bits 0-4
Group 4 Protection on bit 5-7



4-0 These bits specify the number of scan lines in a row. Number of scan lines per row = value + 1.

5 Bit 9 of the Vertical Blank Start register

6 Bit 9 of the Line Compare register

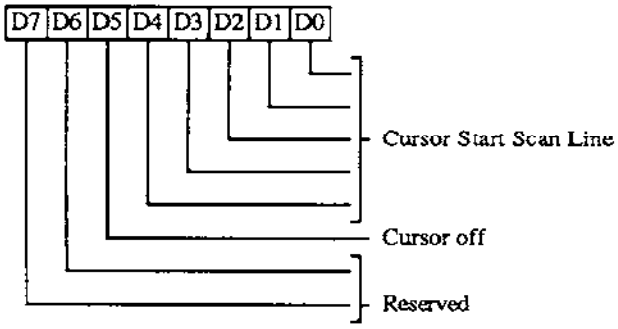
7 Double Scan

0: Normal Operation
1: Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 These bits specify the scan line of the character row where the cursor display begins.

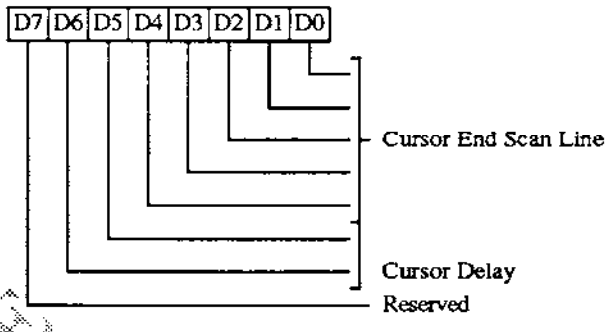
5 Cursor Off

0: Text Cursor On
1: Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 protection



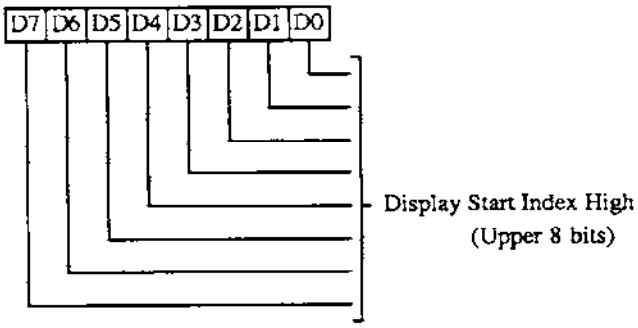
4-0 These bits specify the scan line of a character row where the cursor display ends: Last scan line for the block cursor = Value + 1.

6-5 These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

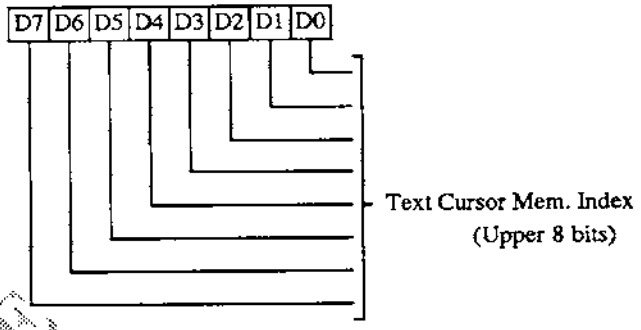
Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

START INDEX HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch



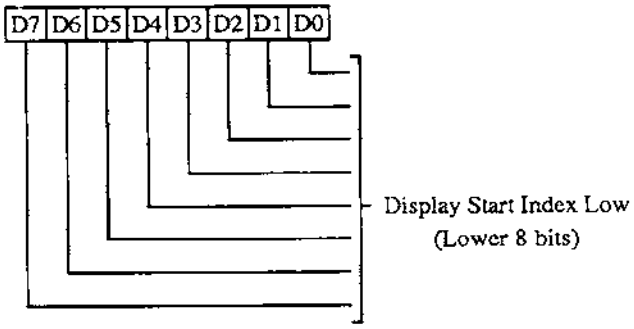
7-0 Upper 8 bits of display start address. In CGA/MDA/Hercules modes, this register wraps around at the 16, 32, and 64 K byte boundaries respectively.

CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh



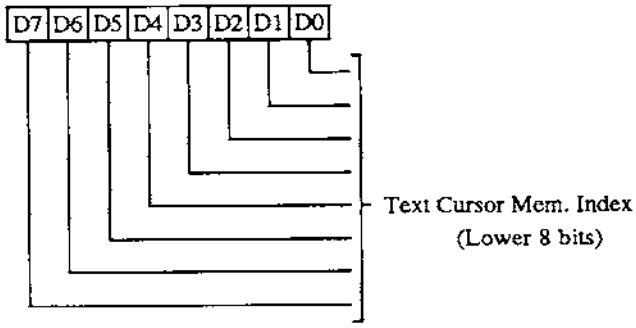
7-0 Upper 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

START INDEX LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh



7-0 Lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Lower 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

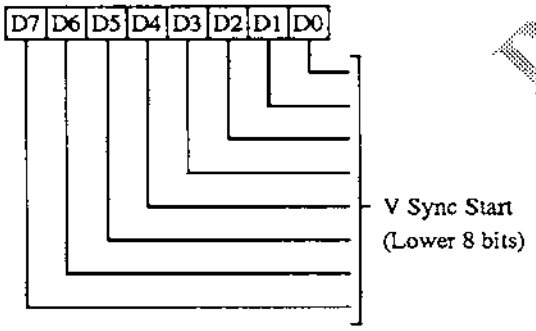
LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

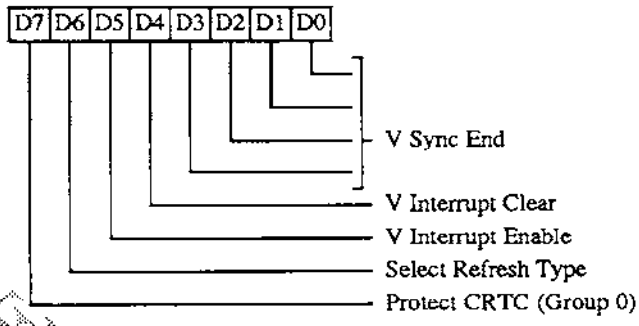
VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection



This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 D7=1.

7-0 The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6 and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03D7=1.

3-0 Vertical Sync End. Lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear. 0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable. 0: Enable vertical interrupt; 1: Disable vertical interrupt. This bit is cleared by RESET.

6 Select Refresh Type:
0: 3 refresh cycles per scan line
1: 5 refresh cycles per scan line

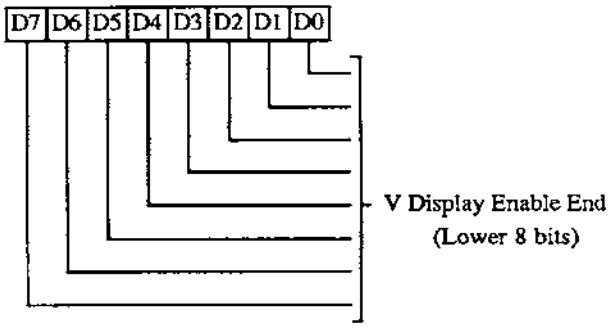
7 Group Protect 0. This bit is logically ORed with XR15D6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0: Enable writes to CR00-CR07
1: Disable writes to CR00-CR07

CR07D4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

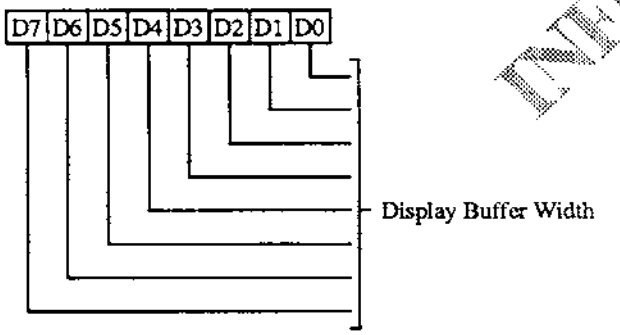
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 protection



7-0 These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)

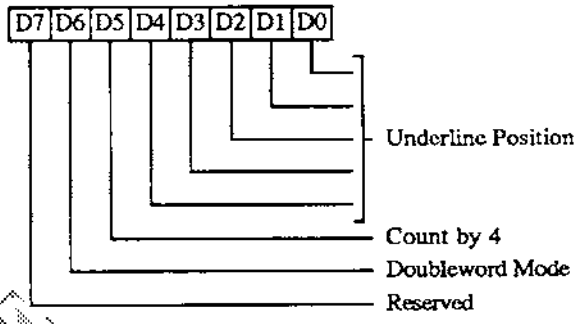
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D and K = 2 in byte mode, K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 protection



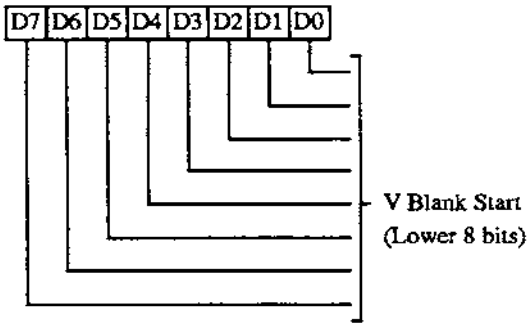
4-0 These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.

5 Count by 4 for Doubleword Mode. 0: Frame Buffer Address is incremented by 1 or 2; 1: Frame Buffer Address is incremented by 4 or 2. See CR17 D3 for further details.

6 Doubleword Mode. 0: Frame Buffer Address is byte or word address; 1: Frame Buffer Address is doubleword address. Used in conjunction with CR17 D6 to select the display memory addressing mode.

7 Reserved (0)

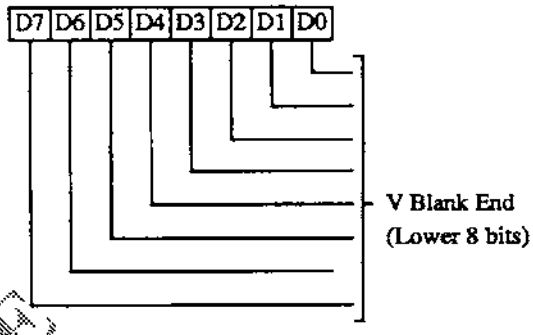
VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 protection



This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 protection

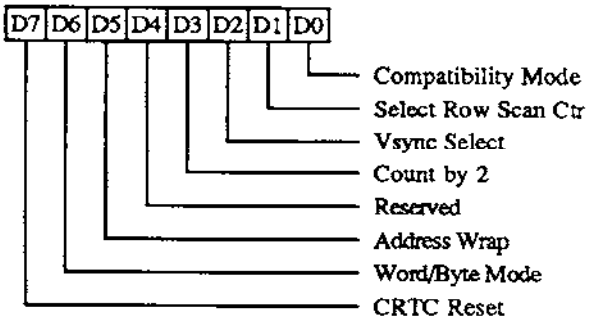


This register is used in all modes.

7-0 End Vertical Blank. These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0,1 and 3-7
Group 4 Protection for bit 2.



0 Compatibility Mode Support. This bit allows compatibility with the IBM CGA two-bank graphics mode. 0: The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time; 1: normal operation, no substitution takes place.

1 Select Row Scan Counter. This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system. 0: Substitute character row scan line counter bit 1 for memory address bit 14 during active display time; 1: normal operation, no substitution takes place.

2 Vertical Sync Select. This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0: Memory address counter is incremented every character clock
1: Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14D5. The net effect is as follows:

CR14 D5	CR17 D3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, the address inrements every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode.)

0: Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode.
1: Normal operation (extended mode).

6 Word Mode or Byte Mode. 0: Word Mode is selected. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output; 1: Select byte mode.

Note: This bit is used in conjunction with CR14 D6 to select byte, word, or double word memory addressing as follows:

CR14 D6	CR17 D6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset (This bit is cleared by RESET)

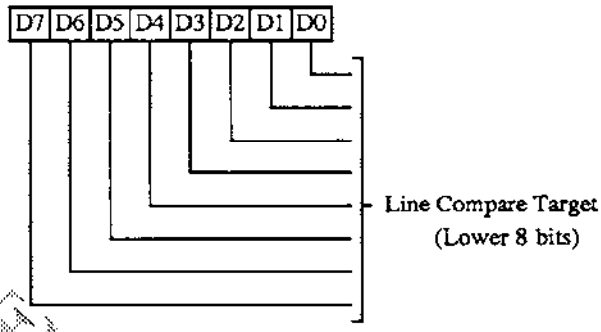
0: Force HSYNC and VSYNC to be inactive. No other registers or outputs affected.
1: Normal Operation.

Display memory addresses are affected by CR17 D6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 D5 + A15 * CR17 D5
Note 2 = A12 xor (A14 * XR04 D2)
Note 3 = A13 xor (A15 * XR04 D2)

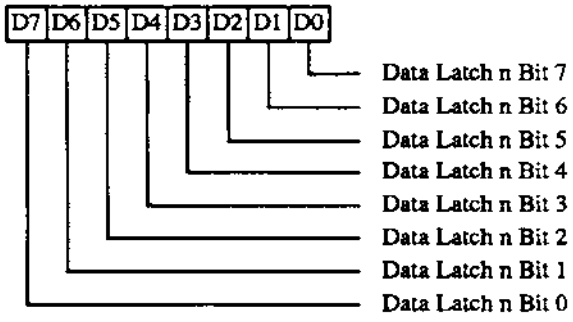
LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 protection



7-0 These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 D7).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



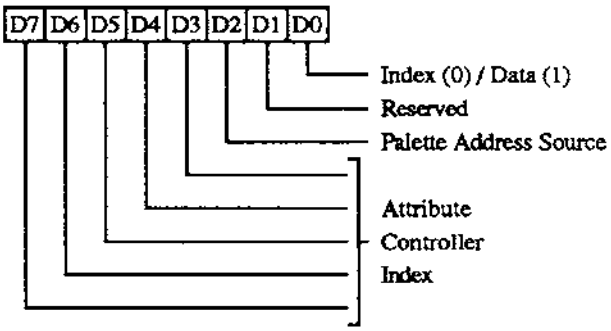
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 D0&1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



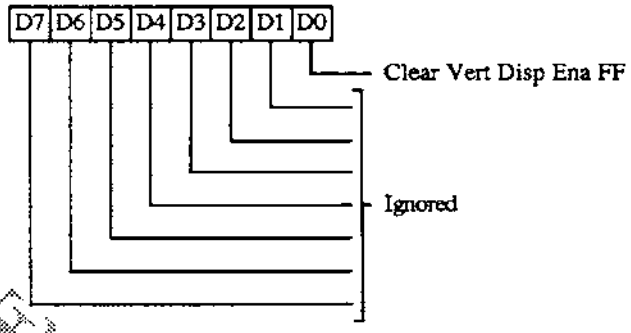
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3X)

Write only at I/O Address 3B5h/3D5h
Index 3xh



Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

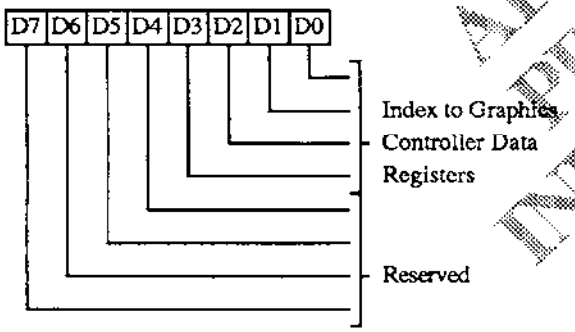
Reads from this register are not decoded and will return indeterminate data.

This is a standard VGA register which was not documented by IBM.

82C450 Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	49
GR00	Set/Reset	00h	RW	3CFh	1	49
GR01	Enable Set/Reset	01h	RW	3CFh	1	50
GR02	Color Compare	02h	RW	3CFh	1	50
GR03	Data Rotate	03h	RW	3CFh	1	51
GR04	Read Map Select	04h	RW	3CFh	1	51
GR05	Graphics mode	05h	RW	3CFh	1	52
GR06	Miscellaneous	06h	RW	3CFh	1	54
GR07	Color Don't Care	07h	RW	3CFh	1	54
GR08	Bit Mask	08h	RW	3CFh	1	55

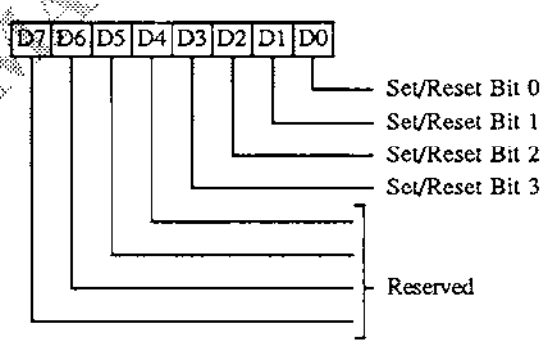
GRAPHICS CONTROLLER INDEX REGISTER (GRX)
Write only at I/O Address 3CEh
Group 1 Protection



3-0 4-bit index to Graphics Controller registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)
Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



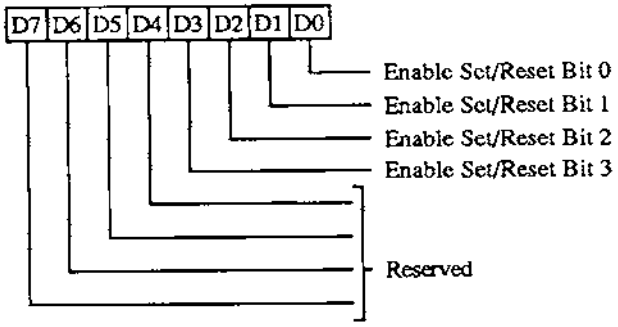
The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

3-0 When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Rest register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

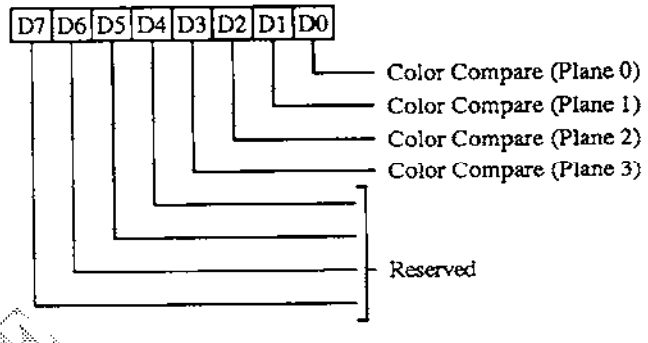
0: The corresponding plane is written with the data from the CPU data bus

1: The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection

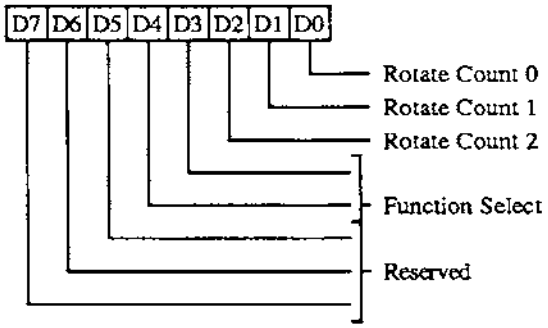


3-0 This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

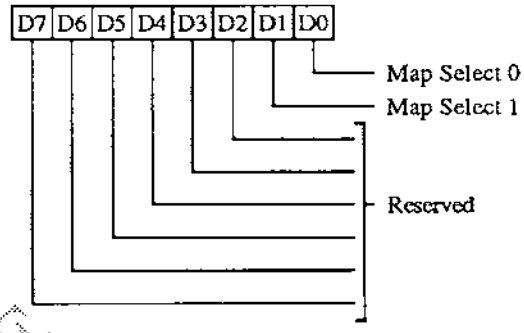
4-3 These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated;
0	1	Logical 'AND' between Data and latched data;
1	0	Logical 'OR' between Data and latched data;
1	1	Logical 'XOR' between Data and latched data.

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

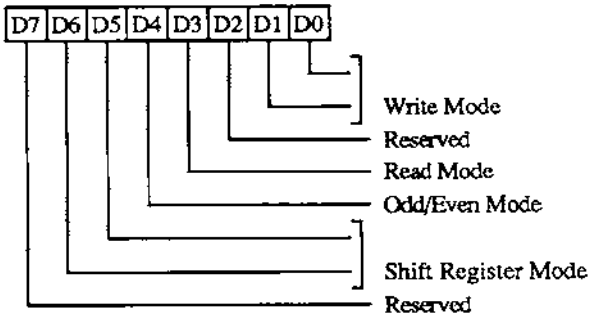
The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 These bits specify the Write Mode as follows: (For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data).

D1	D0	Write Mode
0	0	**Write mode 0.** Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1.** Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2.** The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3.** The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 This bit specifies the Read Mode as follows:

0: The CPU reads data from one of the planes as selected in the Read Map Select register.

1: The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode:

0: All CPU addresses sequentially access all planes

1: Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization.

6-5 Shift Register Mode. These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

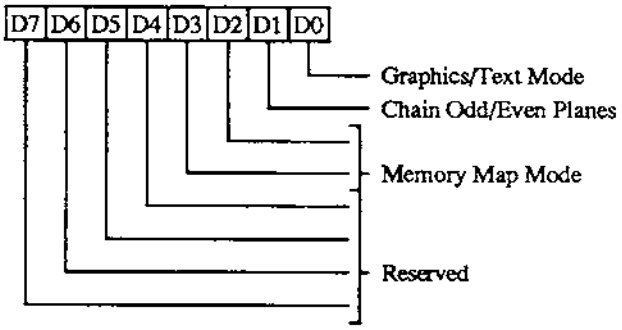
65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D2	M3D6	M2D6	M1D3	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

Note: If the Shift Register is not loaded every character clock (see SR01 D2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode:

0: Text Mode
1: Graphics mode

1 Chain Odd/Even Planes. This mode can be used to double the address space into display memory.

1: CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0: A0 not replaced

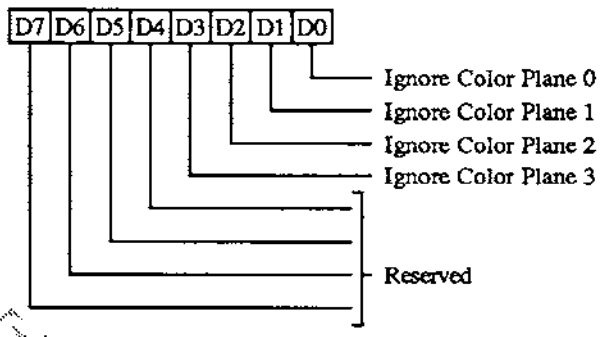
3-2 Memory Map mode. These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



3-0 Ignore Color Plane (0-3):

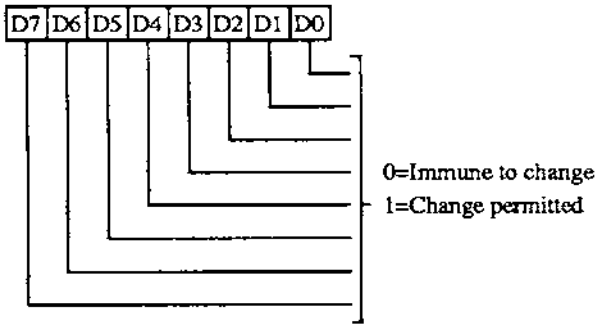
0: This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1: The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)

Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0: The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches.

1: Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

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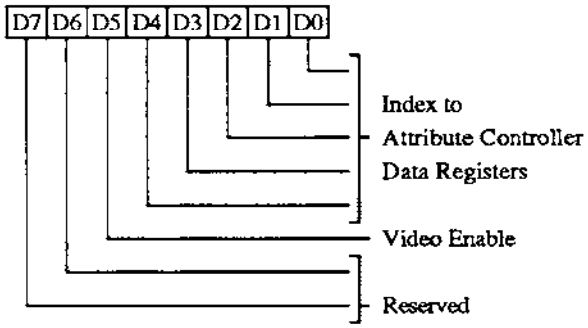
82C450 Attribute Controller and Color Palette Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	57
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	58
AR10	Mode Control	10h	RW	3C0h/3C1h	1	58
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	59
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	59
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	60
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	60
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	61
DACSTATE	DAC State	–	R	3C7h	–	61
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	62
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	62
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	62

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 These bits point to one of the internal registers of the Attribute Controller.

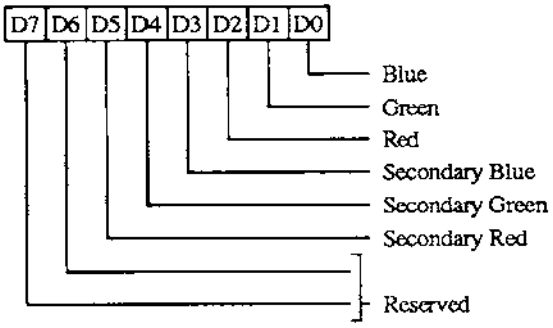
5 Enable Video:

0: Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU

1: Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU.

7-6 Reserved (0)

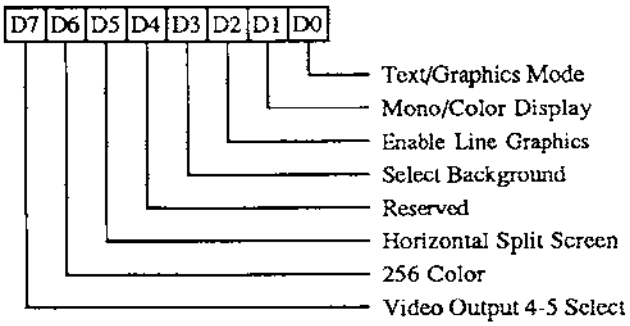
ATTRIBUTE CONTROLLER COLOR PALETTE DATA REGISTERS (AR00-AR0F)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63D6



5-0 These bits are the color value in the respective palette register as pointed to by the index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode:
- 0: Select text mode
- 1: Select graphics mode

1 Monochrome/Color Display
- 0 Select color display attributes
- 1 Select mono display attributes

2 Enable Line Graphics Character Codes. This bit is dependent on bit 0 of the Override register.
- 0: Make the ninth pixel appear the same as the background
- 1: For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity. The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).
- 0: Disable Blinking and enable text mode background intensity
- 1: Enable the blink attribute in text and graphics modes.

4 Reserved (0)

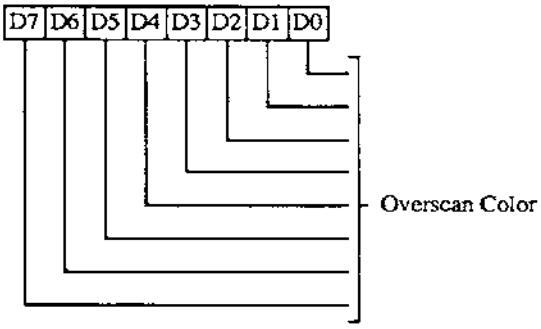
5 Split Screen Horizontal Panning Mode
- 0: Scroll both screens horizontally as specified in the Pixel Panning register
- 1: Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler
- 0: 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock
- 1: Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select:
- 0: Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers
- 1: Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

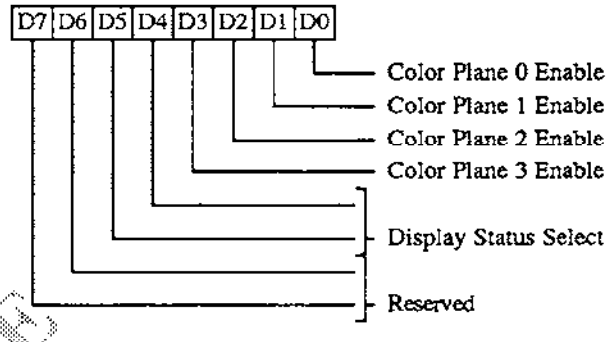


7-0 Overscan Color. These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (0-3) Enable

0: Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1: Enable the plane data bit of the corresponding color plane to pass

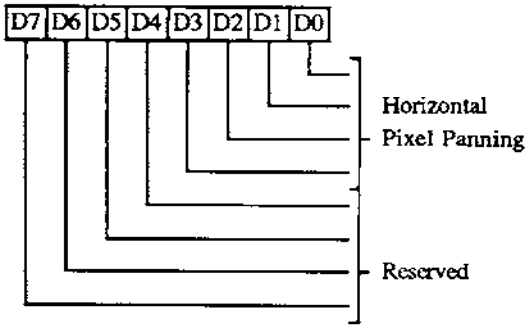
5-4 Display Status Select. These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



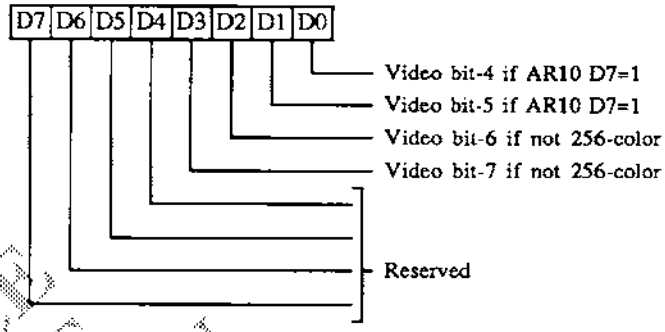
3-0 Horizontal Pixel Panning. These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 D6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection

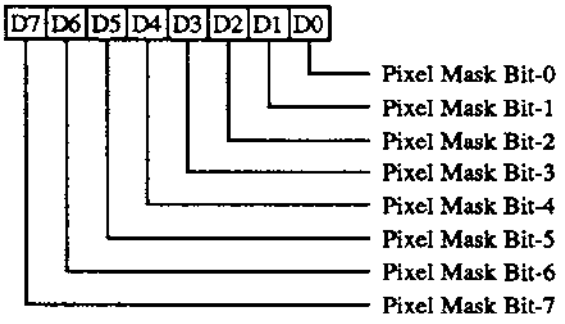


1-0 These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

3-2 These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4 Reserved (0)

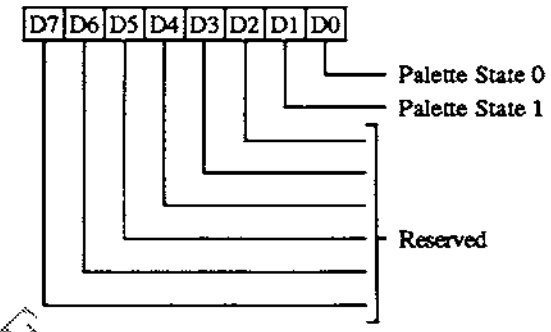
EXTERNAL COLOR PALETTE PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection



The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip (used for displaying analog data to the CRT). Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

EXTERNAL COLOR PALETTE STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h



1-0 Status bits indicate the I/O address of the last CPU write to the external DAC/Color Palette:

00 The last write was to 3C8h (write mode)

11 The last write was to 3C7h (read mode)

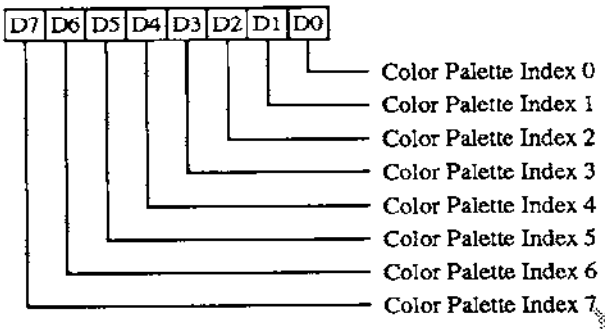
7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.

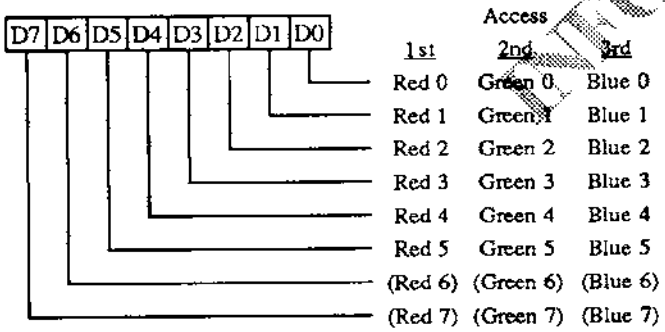
This register is physically located in the 82C450 chip (PALRD/ is *not* asserted for reads from this I/O address).

EXTERNAL COLOR PALETTE READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

EXTERNAL COLOR PALETTE INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



EXTERNAL COLOR PALETTE DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The color palette index and data registers are physically located in the external color palette chip. The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 82C450 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.

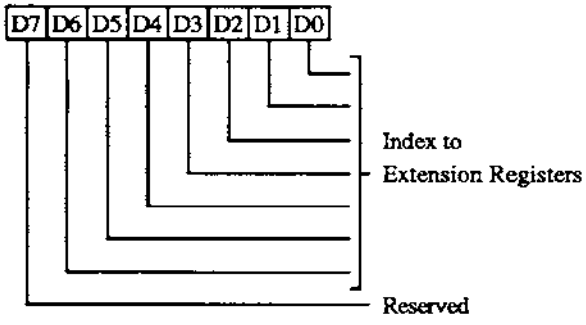
82C450 Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	–	Extension Index	–	RW	3B6h / 3D6h	-xxxxxxx	63
XR00	Misc	Chip Version	00h	R	3B7h / 3D7h	0100rrrr	63
XR01	Misc	Configuration	01h	R	3B7h / 3D7h	dddddddd	65
XR02	Misc	CPU Interface	02h	RW	3B7h / 3D7h	RRRRRRRR	66
XR0D	Misc	Auxiliary Offset	0Dh	RW	3B7h / 3D7h	000000RR	68
XR0E	Misc	Text Mode Control	0Eh	RW	3B7h / 3D7h	0000RR00	68
XR28	Misc	Video Interface	28h	RW	3B7h / 3D7h	00R00RRR	76
XR2B	Misc	Default Video	2Bh	RW	3B7h / 3D7h	RRRRRRRR	76
XR7F	Misc	Diagnostic	7Fh	RW	3B7h / 3D7h	RRxxxxRR	77
XR04	Mapping	Memory Mapping	04h	RW	3B7h / 3D7h	00R0000R	66
XR0B	Mapping	CPU Paging	0Bh	RW	3B7h / 3D7h	000000RR	67
XR0C	Mapping	Start Address Top	0Ch	RW	3B7h / 3D7h	0000000R	67
XR10	Mapping	Single/Low Map	10h	RW	3B7h / 3D7h	xxxxxxxx	69
XR11	Mapping	High Map	11h	RW	3B7h / 3D7h	xxxxxxxx	69
XR14	Compatibility	Emulation Mode	14h	RW	3B7h / 3D7h	RRRRhhRR	70
XR15	Compatibility	Write Protect	15h	RW	3B7h / 3D7h	RRRRRRRR	71
XR1F	Compatibility	Virtual EGA Switch	1Fh	RW	3B7h / 3D7h	R000xxxx	75
XR7E	Compatibility	CGA Color Select	7Eh	RW	3B7h / 3D7h	00xxxxxx	77
XR18	Alternate	Alternate Horizontal Display End	18h	RW	3B7h / 3D7h	xxxxxxxx	72
XR19	Alternate	Alt H Sync Start / Half Line Compare	19h	RW	3B7h / 3D7h	xxxxxxxx	72
XR1A	Alternate	Alternate Horizontal Sync End	1Ah	RW	3B7h / 3D7h	xxxxxxxx	73
XR1B	Alternate	Alternate Horizontal Total	1Bh	RW	3B7h / 3D7h	xxxxxxxx	73
XR1C	Alternate	Alternate Horizontal Blank Start	1Ch	RW	3B7h / 3D7h	xxxxxxxx	74
XR1D	Alternate	Alternate Horizontal Blank End	1Dh	RW	3B7h / 3D7h	Rxxxxxxx	74
XR1E	Alternate	Alternate Offset	1Eh	RW	3B7h / 3D7h	xxxxxxxx	75

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
0 = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
R = Reset to 0 by falling edge of RESET

Note: These registers can be accessed only if enabled through the Extension Enable register (port 103h during setup).

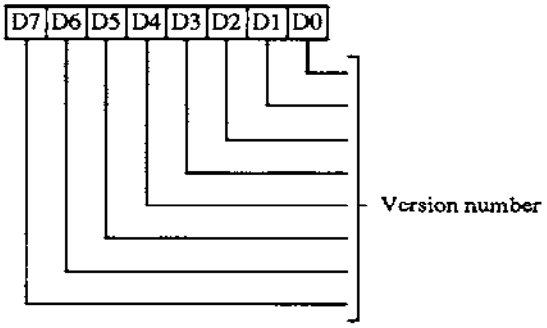
EXTENSION INDEX REGISTER (XRX)
Read/Write at I/O Address 3B6h/3D6h



6-0 Index value used to access the extension registers

7 Reserved (0)

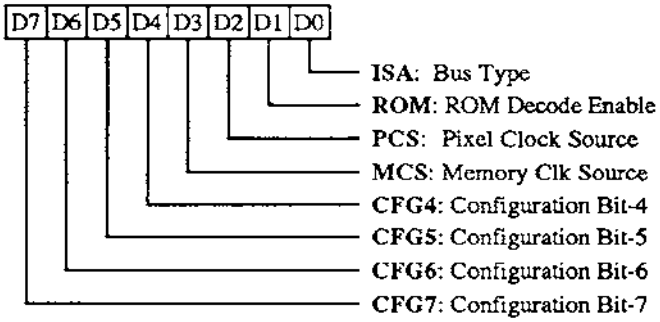
CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3B7h/3D7h
Index 00h



7-0 This register contains the version number for the 82C450. Values start at 40h and are incremented for every silicon step.

CONFIGURATION REGISTER (XR01)

Read only at I/O Address 3B7h/3D7h
Index 01h



These bits latch the state of the CPU data bus (AD bus) on the falling edge of RESET. The state of bits 0-3 after RESET effect the 82C450 internal logic as indicated below; bits 4-7 are latched from AD4-7 on the falling edge of RESET and may be read in this register, but otherwise have no hardware effect on the 82C450 chip. The AD bus has internal on-chip high-valued pullups and will float high if not driven otherwise during RESET so that the default state of all bits is 'one'.

This register is not related to the Virtual EGA Switch register (XR1F).

7-4 **CFG** - Configuration bits: Latched from AD 7-4 at RESET and readable in this register but have no other hardware function.

0 **ISA** - Bus type: 0 = MCA, 1 = ISA

1 **ROM** - ROM Decode Enable: 0 = Disable, 1 = Enable. Setting this bit causes the 82C450 to decode the ROM space (C0000h-C7FFFh) and activate ROMCS/. This bit is valid for ISA Bus only.

2 PCS - Pixel Clock (PCLK) Source

0: CLK0 pin is Memory clock input
CLK1 pin is Pixel clock input
CLK2 pin is CLKSEL0 output
CLK3 pin is CLKSEL1 output

1: CLK0-CLK3 are Pixel clock inputs
CLK0 or CLK1 pin is MCLK input

Note: Actual pixel clock frequencies generated (and how the CLKSEL0-1 outputs are driven) is determined by Misc Output register (MSR) bits 2-3 and/or FCout register (FSR) bits 0-1 (see MCS bit below for clock pin connections and table at bottom of page for actual pixel clock frequencies).

3 MCS - Memory Clock (MCLK) Source

Clock pin connections should be as follows:

External Clock Mux (PCS = 0)

0: MCLK (CLK0) = 56.644 MHz
Clock Select 0 = 40.000 MHz
Clock Select 1 = 50.350 MHz
Clock Select 2 = User-defined
Clock Select 3 = 44.900 MHz

1: MCLK (CLK0) = 50.350 MHz
Clock Select 0 = 40.000 MHz
Clock Select 1 = 28.322 MHz
Clock Select 2 = User-defined
Clock Select 3 = 44.900 MHz

Internal Clock Mux (PCS = 1)

0: CLK0=50.350 MHz
CLK1=56.644 MHz (MCLK source)
CLK2=40.000 MHz
CLK3=44.900 MHz

1: CLK0=50.350 MHz (MCLK source)
CLK1=28.322 MHz
CLK2=40.000 MHz
CLK3=44.900 MHz

Actual internal pixel clock frequencies generated are given in the table below.

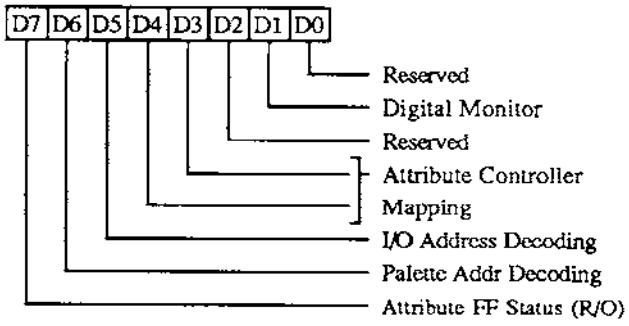
Pixel Clock Frequency Generation

XR02 Bit-1	MSR 3:2	FCR 1:0	PCS = 1 (Int Clk Mux) MCS = 1 (Mclk=50.350) CLK Selected (Pclk Freq)	PCS = 1 (Int Clk Mux) MCS = 0 (Mclk=56.644) CLK Selected (Pclk Freq)	PCS = 0 (Ext Clk Mux)† MCS = 1 (Mclk=50.350) CLKSEL1:0 (Pclk Freq)	PCS = 0 (Ext Clk Mux)† MCS = 0 (Mclk=56.644) CLKSEL1:0 (Pclk Freq)
0	00	xx	CLK0÷2 (25.175 MHz)	CLK0÷2 (25.175 MHz)	xx (MCLK÷2 = 25.175 MHz)	01 (CLKIN÷2 = 25.175 MHz)
1	00	xx	CLK1÷2 (14.161 MHz)	CLK1÷4 (14.161 MHz)	01 (CLKIN÷2 = 14.161 MHz)	xx (MCLK÷4 = 14.161 MHz)
0	01	xx	CLK1 (28.322 MHz)	CLK1÷2 (28.322 MHz)	01 (CLKIN÷1 = 28.322 MHz)	xx (MCLK÷2 = 28.322 MHz)
1	01	xx	CLK0÷3 (16.783 MHz)	CLK0÷3 (16.783 MHz)	xx (MCLK÷3 = 16.783 MHz)	01 (CLKIN÷3 = 16.783 MHz)
x	1x	00	CLK2 (40.000 MHz)	CLK2 (40.000 MHz)	00 (40.000 MHz)	00 (40.000 MHz)
x	1x	01	CLK1 (28.322 MHz)	CLK1 (50.350 MHz)	01 (28.322 MHz)	01 (50.350 MHz)
x	1x	10	CLK0 (50.350 MHz)††	CLK0 (56.644 MHz)††	10 (User-defined)†††	10 (User-defined)†††
x	1x	11	CLK3 (44.900 MHz)	CLK3 (44.900 MHz)	11 (44.900 MHz)	11 (44.900 MHz)

† External clock multiplexing allows the use of an external clock synthesizer chip.
†† Pixel clock frequencies ≥ MCLK are not useful (no memory bandwidth is available for CPU accesses to display memory).
††† An additional user-defined frequency is available by using the external pixel clock multiplexer option.

CPU INTERFACE REGISTER (XR02)

Read/Write at I/O Address 3B7h/3D7h
Index 02h



0 Reserved (0)

1 Digital Monitor clock mode

0: Normal (clock 0-1 = 25 & 28 MHz)
1: Digital Monitor (clk0-1=14 & 16MHz)

14 MHz = 50 MHz ÷ 3
16 MHz = 28 MHz ÷ 2 or 56 ÷ 4

2 Reserved (0)

4-3 Attribute Controller Mapping

4	3	Attribute Controller I/O Mapping
0	0	Write Index and Data at 3C0h (Default on Reset; VGA type mapping).
0	1	Write Index at 3C0h and Data at 3C1h (the attribute flip-flop is always reset in this mode)
1	0	Write Index and Data at 3C0h or 3C1h (EGA type mapping)
1	1	Reserved / Illegal

5 I/O Address Decoding. This bit affects 3B4/5h, 3D4/5h, 3C0-2h, 3C4/5h, 3CE/Fh, 3BAh, 3BFh and 3D8h. 0: Decode all 16 bits of I/O address (Default on Reset); 1: Decode only the lower 10 bits.

6 Palette Address Decoding

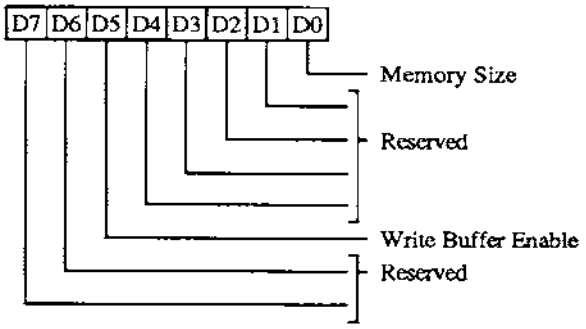
0: Decode 3C6h-3C9h (default)
1: Decode 3C6h-3C9h and 83C6h-83C9h (use for Brooktree-type palette chips)

7 Attribute Flip-flop Status (read only)

0: Index; 1: Data

MEMORY MODE REGISTER (XR04)

Read/Write at I/O Address 3B7h/3D7h
Index 04h



0 Memory Size

0: 256 KBytes of display memory (4 planes of 64K each using two 256Kx4 devices). Default on reset.
1: 512 KBytes of display memory (4 planes of 128K each using four 256Kx4 devices).

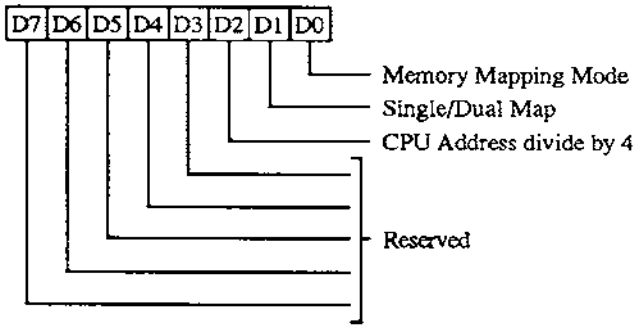
4-1 Reserved (0)

5 Memory Write Buffer

0: Disabled
1: Enabled

7-6 Reserved (0)

CPU PAGING REGISTER (XR0B)
Read/Write at I/O Address 3B7h/3D7h
Index 0Bh



0 Memory Mapping Mode

0: Normal Mode (VGA compatible)
1: Extended Mode (mapping for 512 KByte memory configuration

1 Single/Dual Map

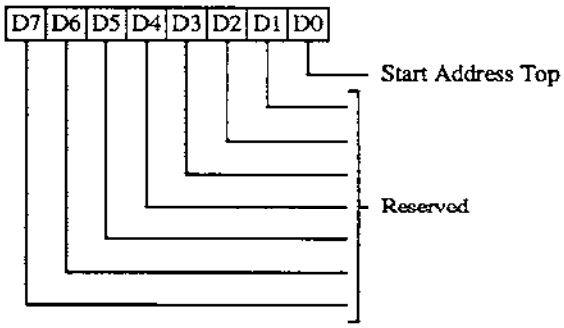
0: CPU uses only a single map to access the extended video memory space. The base address for this map is defined in the Single Map Register (XR10).
1: CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low and High Map Registers (XR10 and XR11)

2 CPU address divide by 4

0: Disable divide by 4 (normal mode)
1: Enable divide by 4 for CPU addresses. This allows video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

7-3 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)
Read/Write at I/O Address 3B7h/3D7h
Index 0Ch

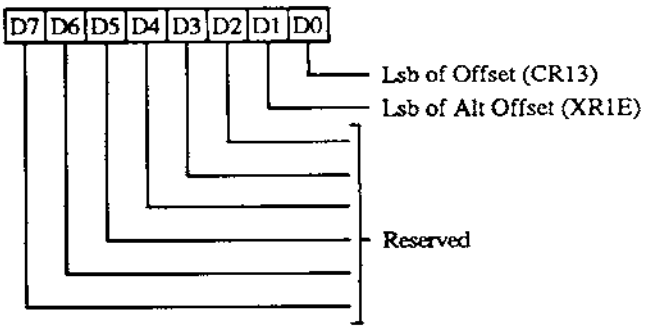


0 Start Address Top. This bit defines the high order bit for the Display Start Address when 512KB of memory is used.

7-1 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3B7h/3D7h
Index 0Dh



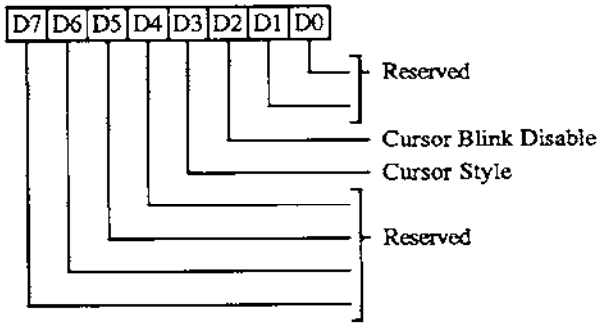
0 This bit provides finer granularity to the Offset when the Chain (Odd/Even) and Chain 4 modes are used. This bit is used with the regular Offset register (CR13).

1 This bit provides finer granularity to the Offset when the Chain (Odd/Even) and Chain 4 modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3B7h/3D7h
Index 0Ch



1-0 Reserved

2 Cursor Blink Disable

0: Blinking
1: Non-blinking

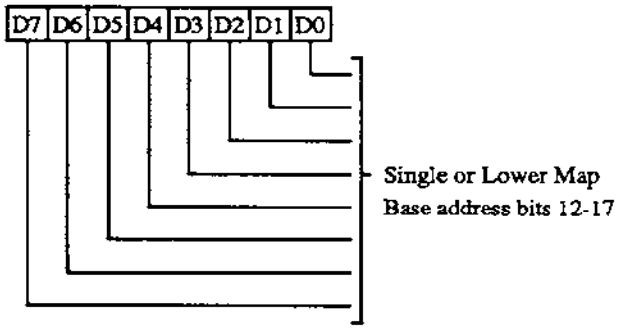
3 Cursor Style

0: Replace
1: Exclusive-Or

7-4 Reserved

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3B7h/3D7h
Index 10h



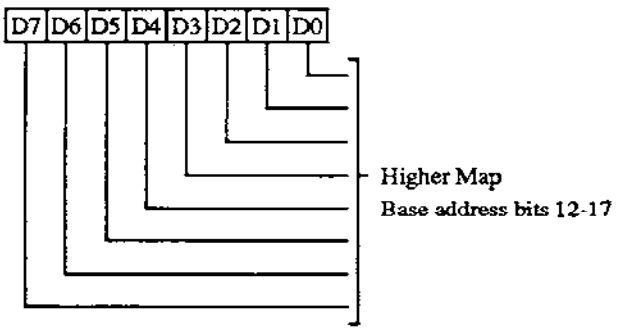
7-0 These eight bits define the Single or Lower Map (in Dual Map Mode) base address bits 17-12. The map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. In case of dual mapping this register controls the CPU window into the display memory based on the contents of GR06 bits 2-3 as follows:

GR06	Low Map
0	0A0000-0AFFFFh
1	0A0000-0A7FFFh
2	0B0000-0B7FFFh
3	0B8000-0BFFFFh

Dual mapping is not allowed in the last two cases. In the last two cases the CPU uses single mapping.

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3B7h/3D7h
Index 11h

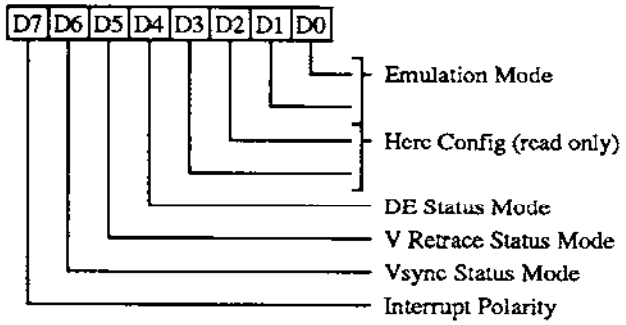


7-0 These eight bits define the Higher Map (in Dual Map Mode) base address bits 17-12. The map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register maps the CPU window into display memory based on the contents of GR06 bits 2-3 as follows:

GR06	Low Map
0	0B0000-0BFFFFh
1	0A8000-0AFFFFh
2	Don't care
3	Don't care

EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3B7h/3D7h
Index 14h



1-0 Emulation Mode

1	0	Mode
0	0	VGA
0	1	CGA
1	0	MDA / Hercules
1	1	EGA

3-2 Hercules Configuration Register (3BFh) readback (read only).

4 Display Enable Status Mode

0: Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

1: Select Hsync status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

5 Vertical Retrace Status Mode

0: Select Vertical Retrace status to appear at bit 3 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

1: Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

6 Vsync Status Mode

0: Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

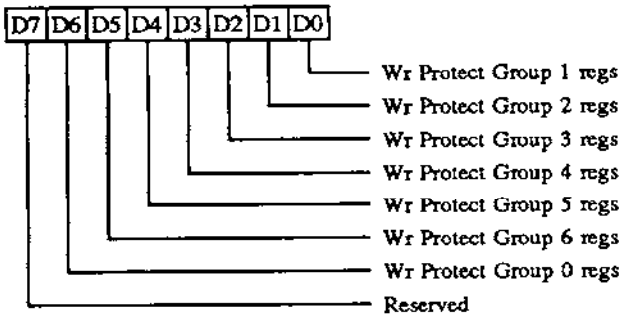
1: Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

7 Interrupt Output Function

This bit controls the function of the IRQ/ output in both MCA-bus and PC-bus.

	XR14[7]=0	XR14[7]=0	
Interrupt State	PC Bus	MCA Bus	XR14[7]=1
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3B7h/3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected, 1= protected.

0 Write Protect Group 1 Registers

Sequencer (SR00-SR04)
Graphics Controller (GR00-GR08)
Attribute Controller (AR00-14)

1 Write Protect Group 2 Registers

Cursor Size register (CR09) bits 0-4
Character Height regs (CR0A, CR0B)

2 Write Protect Group 3 Registers

CRT Controller CR07 bit-4
CRT Controller CR08
CRT Controller CR11 bits 4 and 5
CRT Controller CR13 and CR14
CRT Controller CR17 bits 0,1 & 3-7
CRT Controller CR18

(Split screen, smooth scroll, & CRTC mode control registers)

3 Write Protect Group 4 Registers

CRT Controller CR09 bits 5-7
CRT Controller CR10
CRT Controller CR11 bits 0-3 & 6
CRT Controller CR12, CR15, CR16
CRT Controller CR17 bit-2

4 Write Protect Group 5 Registers

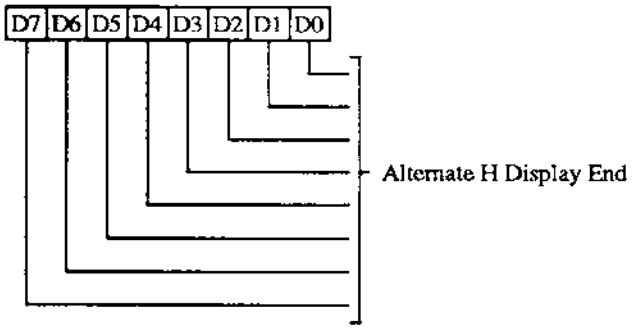
Miscellaneous Output (3C2h)
Feature Control (3BA/3DAh)

5 Write Protect Group 6. (I/O Addresses 3C6-3C9h). The PALRD/ and PALWR/ output signals are disabled and the 82C450 DAC state register is write protected.

6 Write Protect Group 0. Auxiliary Write Protect for CRT Controller registers CR00-CR07 except CR07[4]. This bit is logically ORed with CR11[7].

7 Reserved

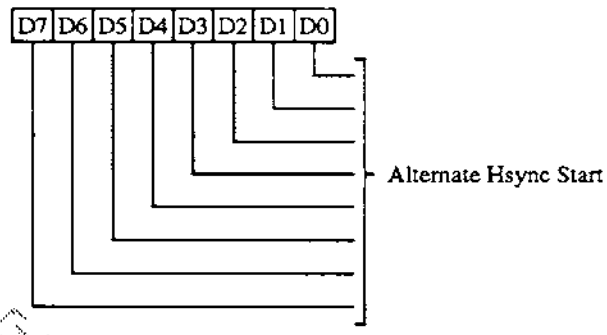
ALTERNATE HORIZONTAL DISPLAY ENABLE END (XR18)
Read/Write at I/O Address 3B7h/3D7h
Index 18h



This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0 Alternate Horizontal Display Enable End. The value in this register defines the number of characters to be displayed per horizontal line. The programmed value is the number of characters displayed per scan line – 1.

ALTERNATE HORIZONTAL SYNC START / HALF LINE COMPARE (XR19)
Read/Write at I/O Address 3B7h/3D7h
Index 19h



This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

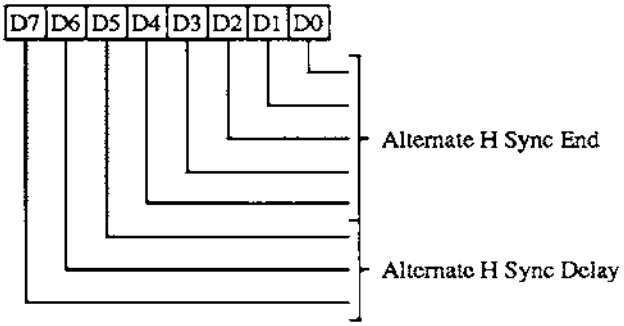
7-0 Alternate Horizontal Sync Start or Half Line Compare.

XR28 bit-3 = 0 (Non-interlaced Video)
When the alternate register set is in effect, the value in this register defines the beginning of Horizontal Sync in terms of character clocks from the beginning of the display scan. This controls the centering of the display on the screen.

XR28 bit-3 = 1 (Interlaced Video)
The value in this register is used to generate the 'half-line compare' signal that controls the positioning of the Vsync for odd frames.

ALTERNATE HORIZONTAL SYNC END (XR1A)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ah



This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

4-0 Alternate Horizontal Sync End. Lower 5 bits of the character count that defines the end of Horizontal Sync.

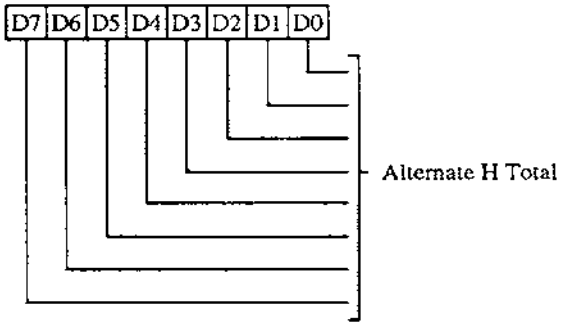
The value programmed into bits 0-4 of this register is the lower 5 bits of the sum of the value in Horizontal Sync Start register plus the desired Horizontal Sync Width.

6-5 Alternate Horizontal Sync Delay. The value in these bits defines the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Alternate Horizontal Blank End bit-5. Sixth bit of the Horizontal Blank End register (CR03).

ALTERNATE HORIZONTAL TOTAL (XR1B)

Read/Write at I/O Address 3B7h/3D7h
Index 1Bh

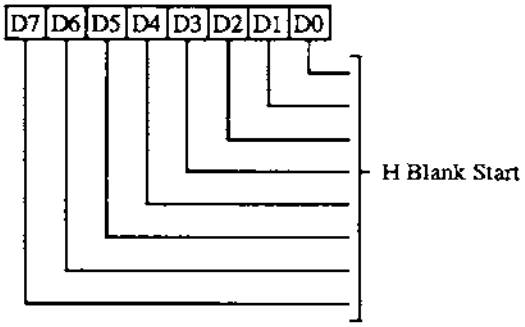


This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0 Alternate Horizontal Total. This register defines the total number of character times in a scan line including both displayed characters and retrace. The programmed value is the number of character clocks per scan line minus 5 for VGA mode and minus 2 for EGA mode.

ALTERNATE HORIZONTAL BLANK START (XR1C)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ch

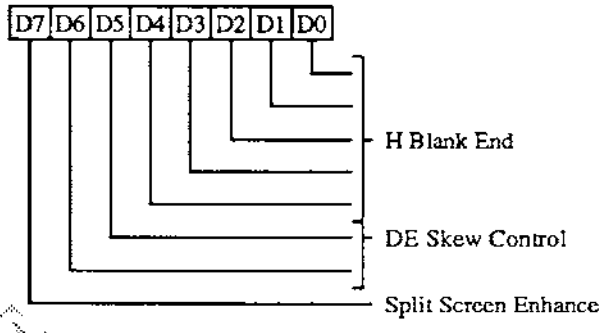


This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0 Alternate Horizontal Blank Start. This register defines the beginning of Horizontal Blanking in terms of character clocks. The period between horizontal display enable end and horizontal blanking start is the right side border on the screen.

ALTERNATE HORIZONTAL BLANK END (XR1D)

Read/Write at I/O Address 3B7h/3D7h
Index 1Dh



This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

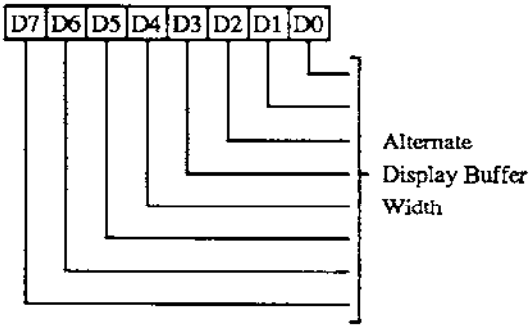
4-0 Alternate Horizontal Blank End. These bits are programmed with the lower 5 bits of the character count that defines the end of horizontal blanking. The interval between the end of horizontal blanking and the beginning of the display (count 0) is the left side border on the screen. The programmed value is calculated by adding the value in the horizontal blanking start register to the desired horizontal blanking width. The lower 5 bits of the result is programmed into this register and the sixth bit is programmed into CR05.

6-5 Display Enable Skew Control. These bits define the number of character clocks (0-3) that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Split Screen Enhancement

0: IBM VGA compatible operation
1: Enhances split-screen functionality. Also, this bit should be set to '1' for Hercules graphics mode (720x348 resolution).

ALTERNATE OFFSET (XR1E)
Read/Write at I/O Address 3B7h/3D7h
Index 1Eh



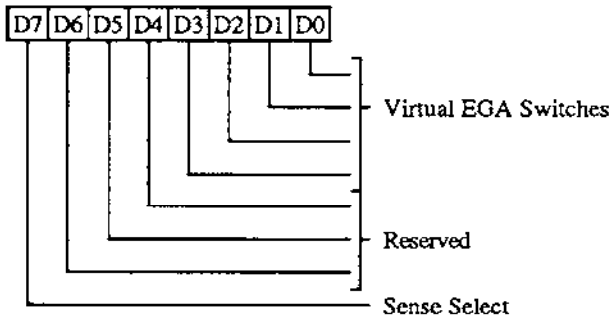
This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0 Alternate Offset. The byte starting address of the next display row is 'Byte start address of the current row plus (K times the contents of the Offset Register)' where K = 2 in byte mode and 4 in word mode.

To provide finer granularity in offset, an additional bit is defined in the Auxiliary Offset Register in the extended I/O space. This additional bit essentially adds a least significant bit to the Offset.

The byte or word mode for the memory address is selected by the CRT mode control Register bit-6. The 400-line register bit-2 allows byte/word resolution to the display buffer width.

VIRTUAL SWITCH REGISTER (XR1F)
Read/Write at I/O Address 3B7h/3D7h
Index 1Fh



3-0 Virtual switch register bits 3-0. If bit-7 of this register is '1', then one of these four bits is read back in Input Status Register 0 bit-4. The bit selected is determined by Misc Output Register (3C2h) bits 2-3.

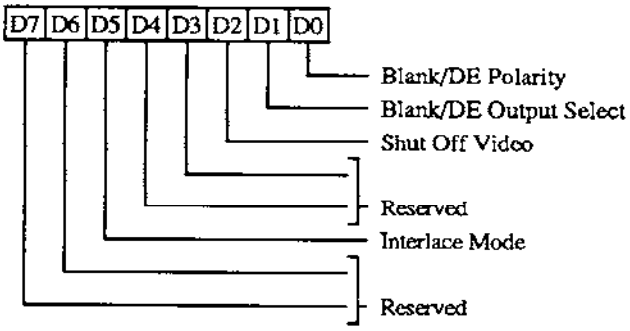
6-4 Reserved (0)

7 Sense Select

0: Select the SENSE pin for readback in Input Status Register 0 bit-4.

1: Select one of bits 0-3 of this register for readback in Input Status Register 0 bit-4.

VIDEO INTERFACE REGISTER (XR28)
Read/Write at I/O Address 3B7h/3D7h
Index 28h



0 BLANK/Display Enable Polarity

0: Negative
1: Positive

1 Blank / Display Enable Select

0: BLANK/ pin outputs BLANK/
1: BLANK/ pin outputs DE

The signal polarity selected by bit 0 is applicable for either selection.

2 Shut off Video

0: Video forced to 00 (Default Video Register) during blank time.
1: Video forced to default video when the screen is blanked

4-3 Reserved (0)

5 Interlace Mode

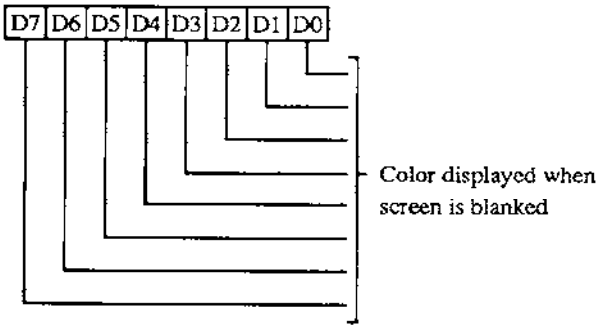
0: Non-interlaced video
1: Interlaced video

In interlace mode, XR19 holds the half-line compare value which controls the positioning of Vsync for odd frames.

Note: Interlace may be used in graphics modes only.

7-6 Reserved (0)

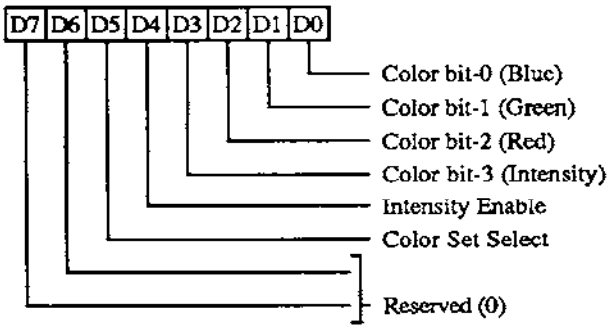
DEFAULT VIDEO REGISTER (XR2B)
Read/Write at I/O Address 3B7h/3D7h
Index 2Bh



7-0 These bits specify the color to be displayed when the screen is forced to the blank state using SR1 bit-5.

CGA COLOR SELECT (XR7E)

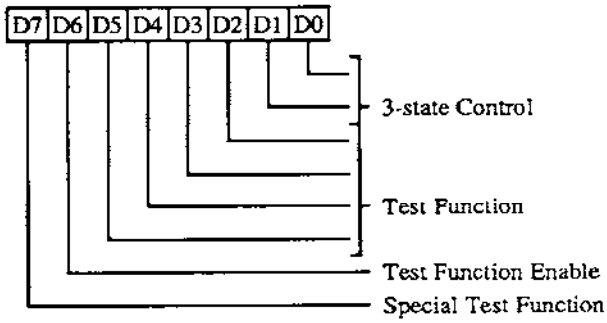
Read/Write at I/O Address 3B7h/3D7h
Index 7Eh



This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode. The copy at XR7E is always visible.

DIAGNOSTIC (XR7F)

Read/Write at I/O Address 3B7h/3D7h
Index 7Fh



0 3-state control bit-0

0: Normal outputs (default)
1: 3-state the following pins:

PALRD/, PALWR/,
RDY, IRQ,
HSYNC, VSYNC

1 3-state control bit-1

0: Normal outputs (default)
1: 3-state the following pins:

WE/,
RASA/, RASB/,
CASA/, CASB/,
AA8[8:0], BA8[8:0]

5-2 Test Function bits. These bits select one of sixteen functions used for internal testing of the 82C450 chip.

6 Test Function Enable. Used to enable one of sixteen functions selected by bits 5-2. This bit should be set to 0 for normal operation (default on reset).

7 Special Test Function. Prevents CPU data bus collision problems with certain manufacturing vendors. This bit should be set to 0 for normal operation (default on reset).

All bits in this register should be set to '0' for normal operation. On power up (RESET) all bits default to '0'.

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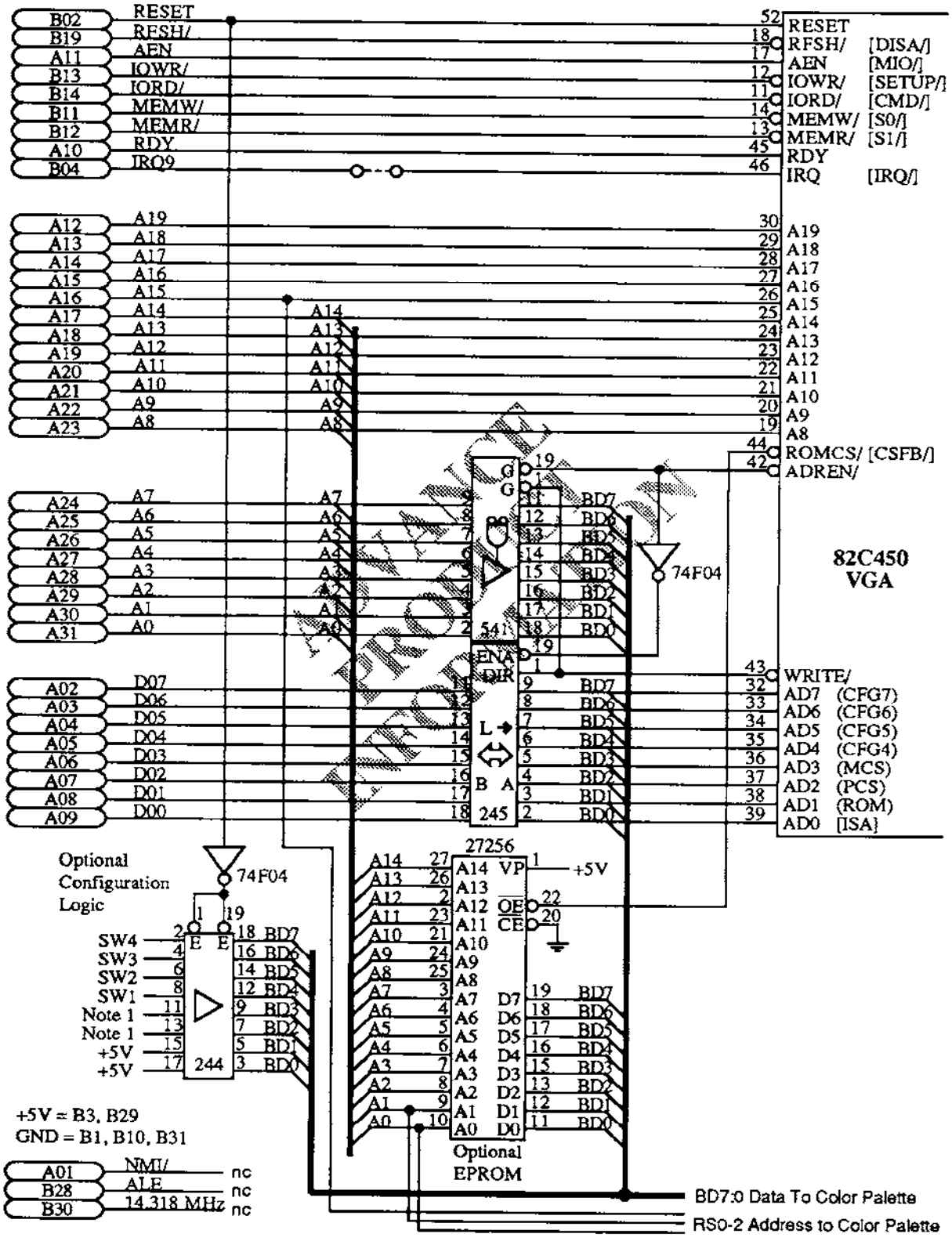
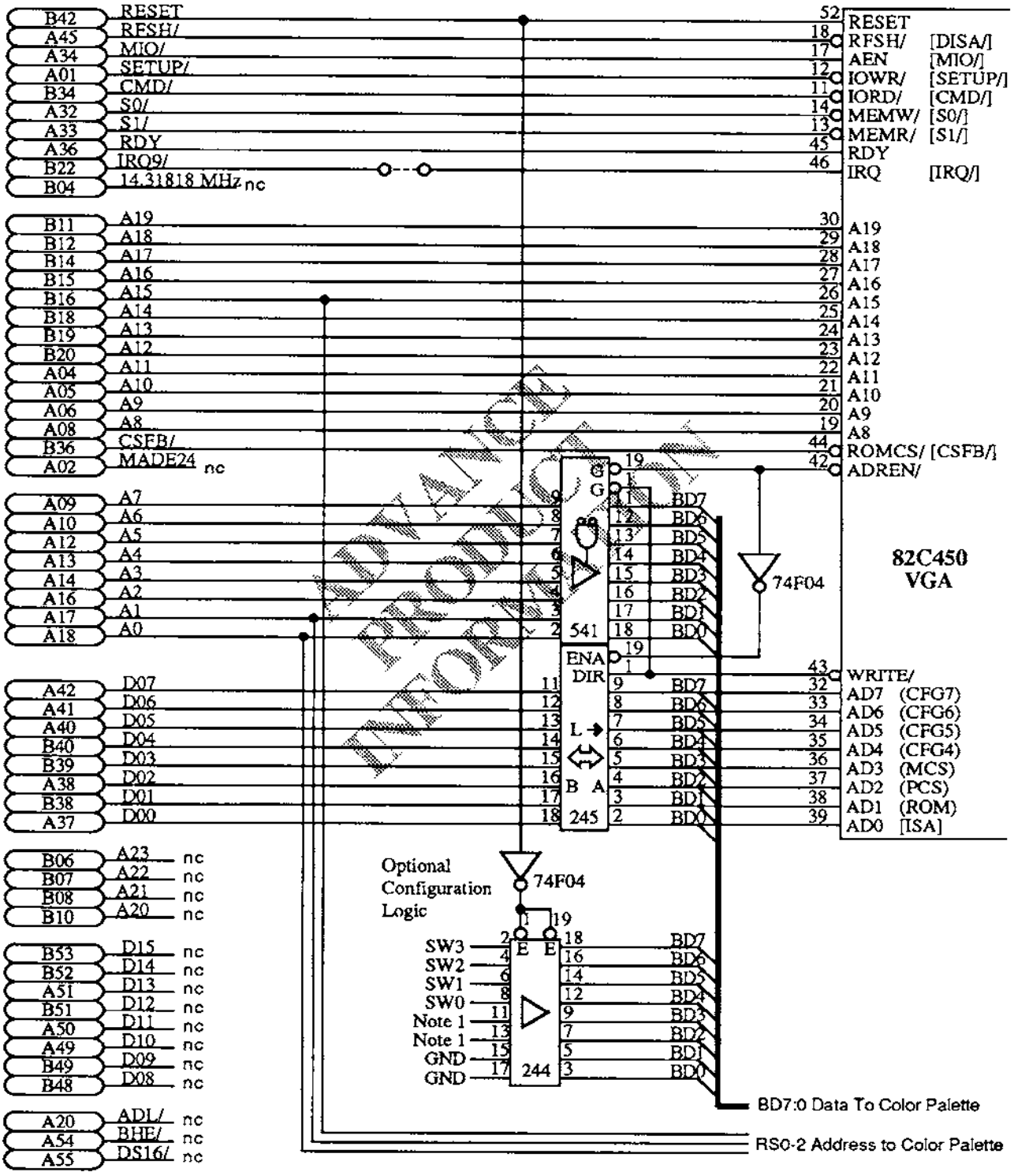
82C450 Application Schematic Examples

This section includes schematic examples showing how to connect the 82C450 chip. The schematics are broken down into four main groups for discussion:

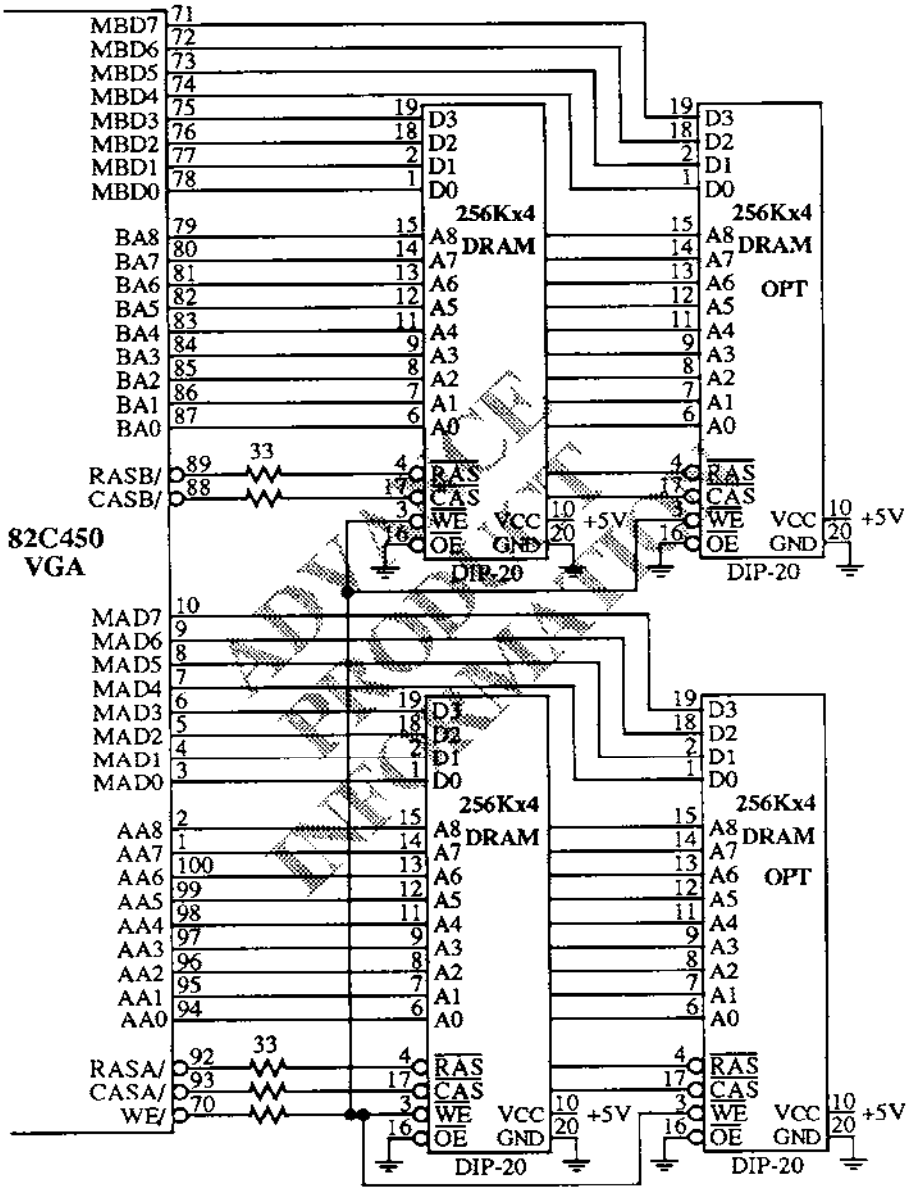
1) System Bus Interface
2) Display Memory Interface
3) Video Interface
4) Clock Interface



82C450 EISA/ISA Bus Circuit Example

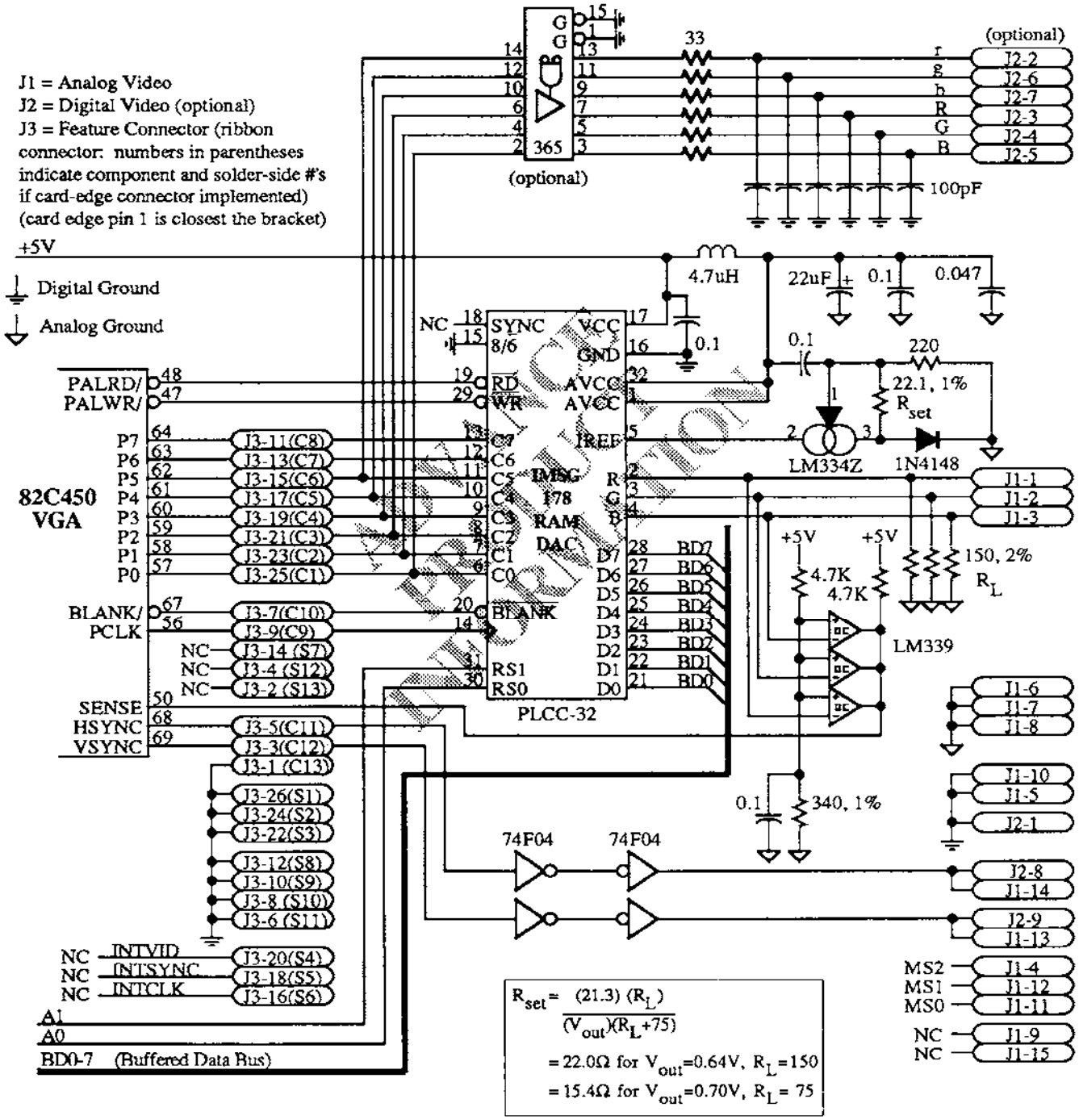


82C450 MCA Bus Circuit Example

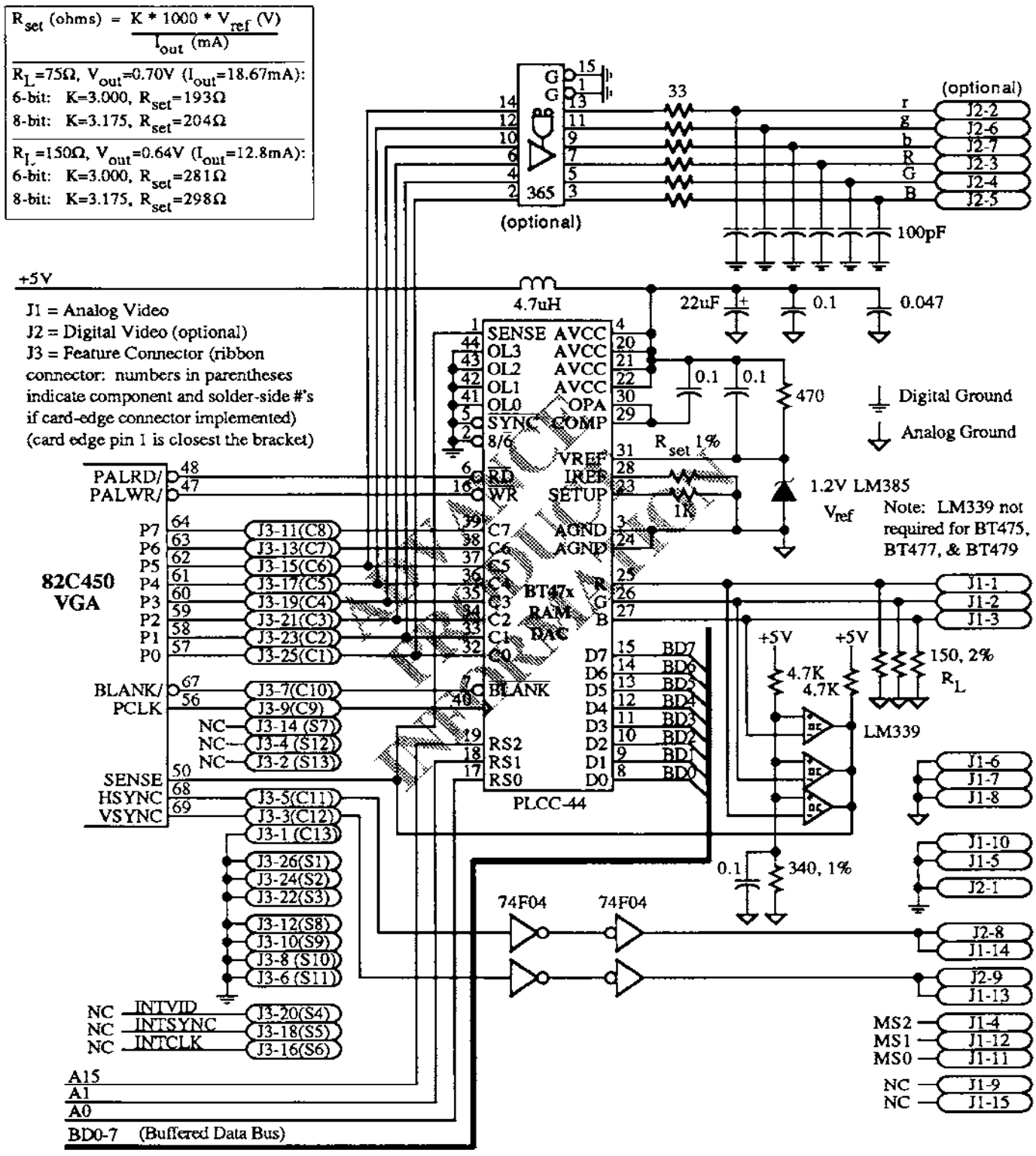


82C450 Display Memory Circuit

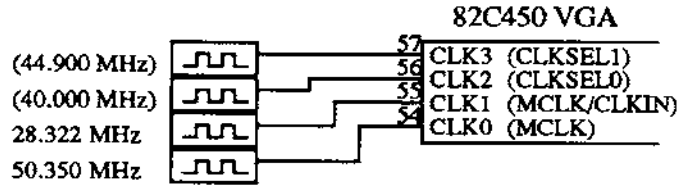
Note: For minimum configurations, two DRAMs may be implemented instead of four. In this case, the two optional DRAMs on the right side of the above circuit marked 'OPT' may be removed.



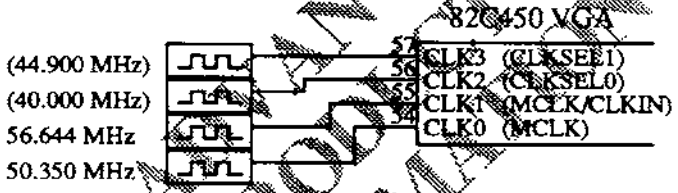
82C450 Video Circuit Example - External Color Palette (Inmos IMSG176 / 178)



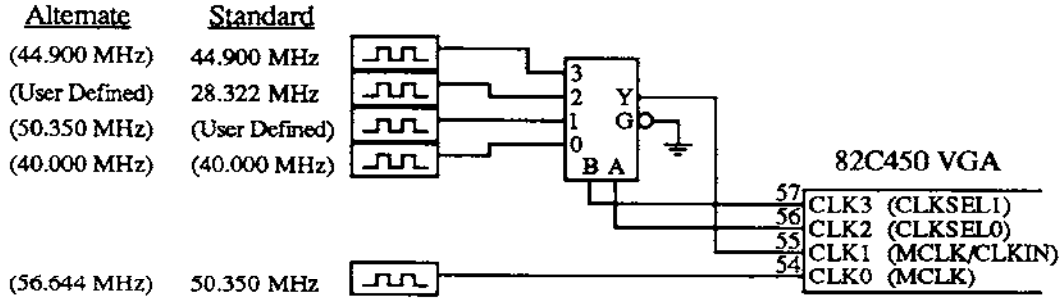
82C450 Video Circuit Example - External Color Palette (Brooktree BT471 / 478)



82C450 Clock Circuit Example 1 - Minimum Configuration 1



82C450 Clock Circuit Example 2 - Minimum Configuration 2



82C450 Clock Circuit Example 3 - Alternate Configuration (External Clock Multiplexer)

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82C450 Electrical Specifications

82C450 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C450 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Ambient Temperature	0	–	55	°C

82C450 DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CC1}	Power Supply Current	@25 MHz CLK, 0°C	–	65	100	mA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage		–0.5	–	0.8	V
V_{IH}	Input High Voltage	All pins except clocks	2.0	–	V_{CC}+0.5	V
		CLK0, CLK1, CLK2, CLK3	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (RDY, IRQ)	–	–	0.45	V
		I_{OL} = 2 mA (MAD,MBD,AA,BA)	–	–	0.45	V
		I_{OL} = 4 mA (all others)	–	–	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –8 mA (RDY, IRQ)	2.4	–	–	V
		I_{OH} = –2 mA (MAD,MBD,AA,BA)	2.4	–	–	V
		I_{OH} = –4 mA (all others)	2.4	–	–	V

Electrical specifications contained herein are preliminary and subject to change without notice.

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82C450 Mechanical Specifications