

DATA SHEET

~~74F175*~~, 74F175A Quad D flip-flop

** Discontinued part. Please see the Discontinued Product List in Section 1, page 21.*

Product specification

1996 Mar 12

IC15 Data Handbook

Quad D flip-flop

74F175A

FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (-40°C to $+85^{\circ}\text{C}$)
- PNP light loading inputs

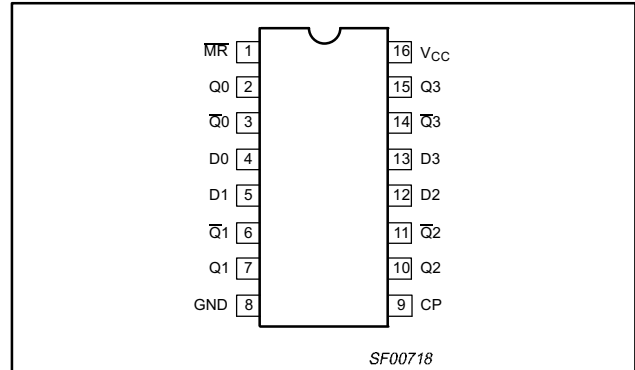
DESCRIPTION

The 74F175A is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where both true and complementary outputs are required, and the CP and $\overline{\text{MR}}$ are common to all storage elements.

PIN CONFIGURATION



| TYPE | TYPICAL f_{max} | TYPICAL SUPPLY CURRENT (TOTAL) |
|---------|--------------------------|--------------------------------|
| 74F175A | 160MHz | 22mA |

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | PKG. DWG. # |
|--------------------|---|-------------|
| | COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$, $T_{\text{amb}} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ | |
| 16-pin plastic DIP | 74F175AN | SOT38-4 |
| 16-pin plastic SO | 74F175AD | SOT109-1 |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-------------------------|----------------------------------|---------------------|---------------------|
| D0 – D3 | Data inputs | 74F175A | 1.0/0.033 |
| $\overline{\text{MR}}$ | Master reset input (active–Low) | 74F175A | 1.0/0.033 |
| CP | Clock input (active rising edge) | 74F175A | 1.0/0.033 |
| Q0–Q3 | True outputs | | 50/33 |
| $\bar{Q}0$ – $\bar{Q}3$ | Complementary outputs | | 50/33 |

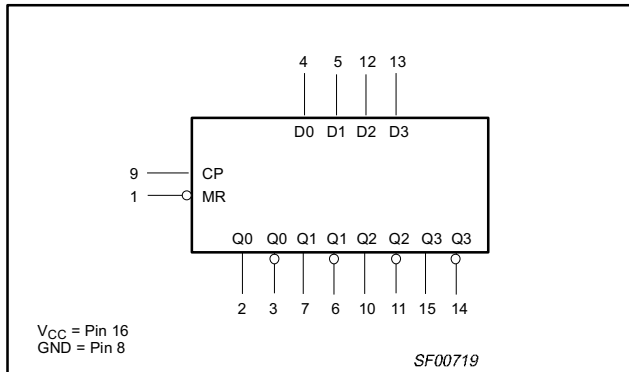
NOTE:

One (1.0) FAST unit load is defined as: $20\mu\text{A}$ in the High state and 0.6mA in the Low state.

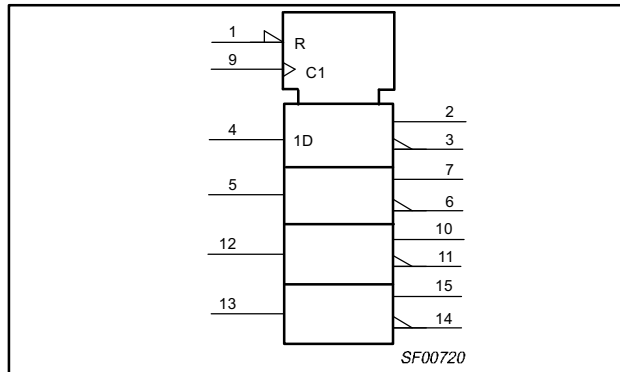
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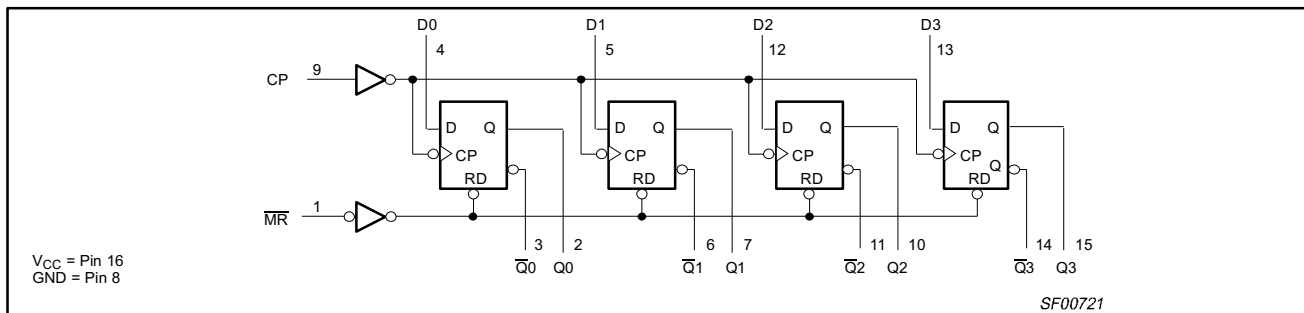
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

| INPUTS | | | OUTPUTS | | OPERATING MODE |
|--------|----|----------------|----------------|-------------|----------------|
| MR | CP | D _n | Q _n | \bar{Q}_n | |
| L | X | X | L | H | Reset (clear) |
| H | ↑ | h | H | L | Load "1" |
| H | ↑ | l | L | H | Load "0" |

- H = High voltage level
- h = High state must be present one setup time before the Low-to-High clock transition
- L = Low voltage level
- l = Low state must be present one setup time before the Low-to-High clock transition
- X = Don't care
- ↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|-------------------------|---------------|
| V _{CC} | Supply voltage | -0.5 to +7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +5 | mA |
| V _{OUT} | Voltage applied to output in High output state | -0.5 to V _{CC} | V |
| I _{OUT} | Current applied to output in Low output state | 40 | mA |
| T _{amb} | Operating free air temperature range | Commercial range | 0 to +70 °C |
| | | Industrial range | -40 to +85 °C |
| T _{stg} | Storage temperature range | -65 to +150 | °C |

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|------------------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -1 | mA |
| I_{OL} | Low-level output current | | | 20 | mA |
| T_{amb} | Operating free air temperature range | Commercial range | 0 | +70 | °C |
| | | Industrial range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|----------|---|--|------------------|------------------|------|---------------|----|
| | | | MIN | TYP ² | MAX | | |
| V_{OH} | High-level output voltage | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$ | $\pm 10\%V_{CC}$ | 2.5 | | V | |
| | | | $\pm 5\%V_{CC}$ | 2.7 | 3.4 | | |
| V_{OL} | Low-level output voltage | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$ | $\pm 10\%V_{CC}$ | | 0.30 | 0.5 | V |
| | | | $\pm 5\%V_{CC}$ | | 0.30 | 0.5 | |
| V_{IK} | Input clamp voltage | $V_{CC} = \text{MIN}, I_I = I_{IK}$ | | -0.73 | -1.2 | V | |
| I_I | Input current at maximum input voltage | $V_{CC} = 0.0V, V_I = 7.0V$ | | | 100 | μA | |
| I_{IH} | High-level input current | $V_{CC} = \text{MAX}, V_I = 2.7V$ | | | 20 | μA | |
| I_{IL} | Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.5V$ | 74F175A | | -20 | μA | |
| I_{OS} | Short-circuit output current ³ | $V_{CC} = \text{MAX}$ | | -60 | -150 | mA | |
| I_{CC} | Supply current (total) | $V_{CC} = \text{MAX}$ | 74F175A | | 22 | 31 | mA |

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F175A

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | |
|------------------------|-------------------------------------|----------------|--|-----|-----|--|------|--|------|-----|
| | | | $T_{amb} = 25^\circ\text{C}$ $V_{CC} = +5V$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | | $T_{amb} = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| f_{max} | Maximum clock frequency | Waveform 1 | 140 | 160 | | 125 | | 110 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP to Qn or Qn | Waveform 1 | 3.0 | 4.0 | 6.5 | 2.5 | 7.5 | 2.5 | 8.0 | ns |
| | | | 4.5 | 6.0 | 8.5 | 4.0 | 9.0 | 4.0 | 10.0 | |
| t_{PLH} t_{PHL} | Propagation delay MR to Qn | Waveform 3 | 4.5 | 6.5 | 9.0 | 4.5 | 10.0 | 4.5 | 11.0 | ns |
| | | | 4.5 | 6.0 | 8.0 | 4.0 | 9.0 | 4.0 | 10.0 | |

Quad D flip-flop

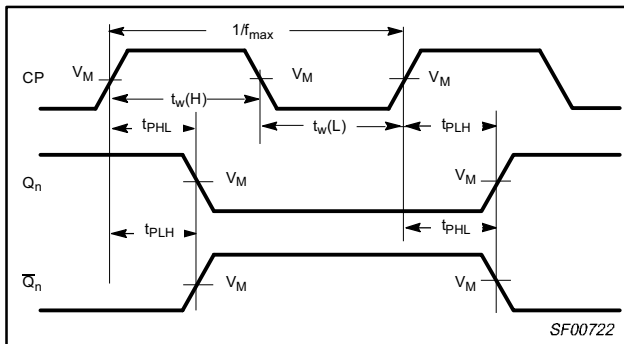
74F175A

AC SETUP REQUIREMENTS FOR 74F175A

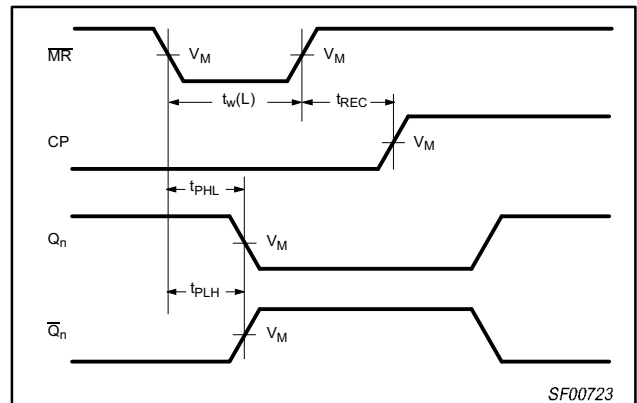
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | | |
|----------------------|----------------------------------|----------------|--|-----|-----|---|-----|---|------------|-----|----|
| | | | $T_{amb} = 25^{\circ}C$ $V_{CC} = +5V$ $C_L = 50pF$, $R_L = 500\Omega$ | | | $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$ | | $T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$, $R_L = 500\Omega$ | | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX | |
| $t_s(H)$ $t_s(L)$ | Setup time, High or Low Dn to CP | Waveform 2 | 3.0 3.0 | | | 3.5 3.5 | | | 4.0 4.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, High or Low Dn to CP | Waveform 2 | 0.0 0.0 | | | 0.0 0.0 | | | 0.0 0.0 | | ns |
| $t_w(H)$ $t_w(L)$ | CP Pulse width High or Low | Waveform 1 | 3.0 4.0 | | | 3.5 5.0 | | | 4.0 5.5 | | ns |
| $t_w(L)$ | MR Pulse width Low | Waveform 3 | 3.5 | | | 3.5 | | | 4.0 | | ns |
| t_{REC} | Recovery time MR to CP | Waveform 3 | 4.0 | | | 4.5 | | | 5.0 | | ns |

AC WAVEFORMS

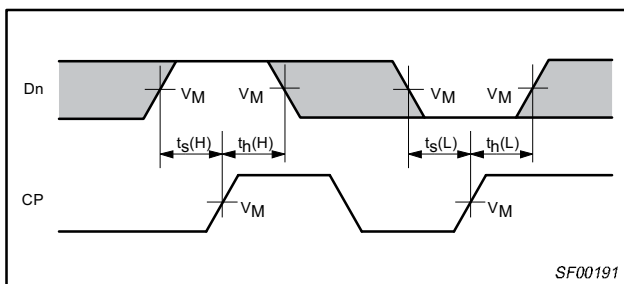
For all waveforms, $V_M = 1.3V$.



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

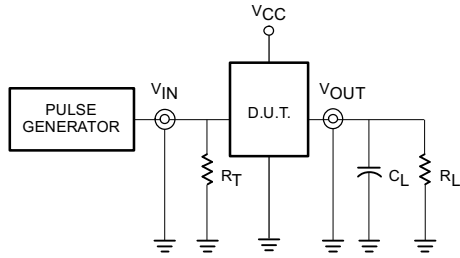


Waveform 2. Data setup time and hold times

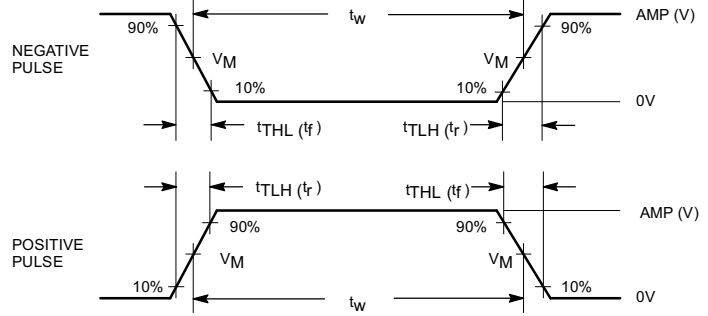
Quad D flip-flop

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TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

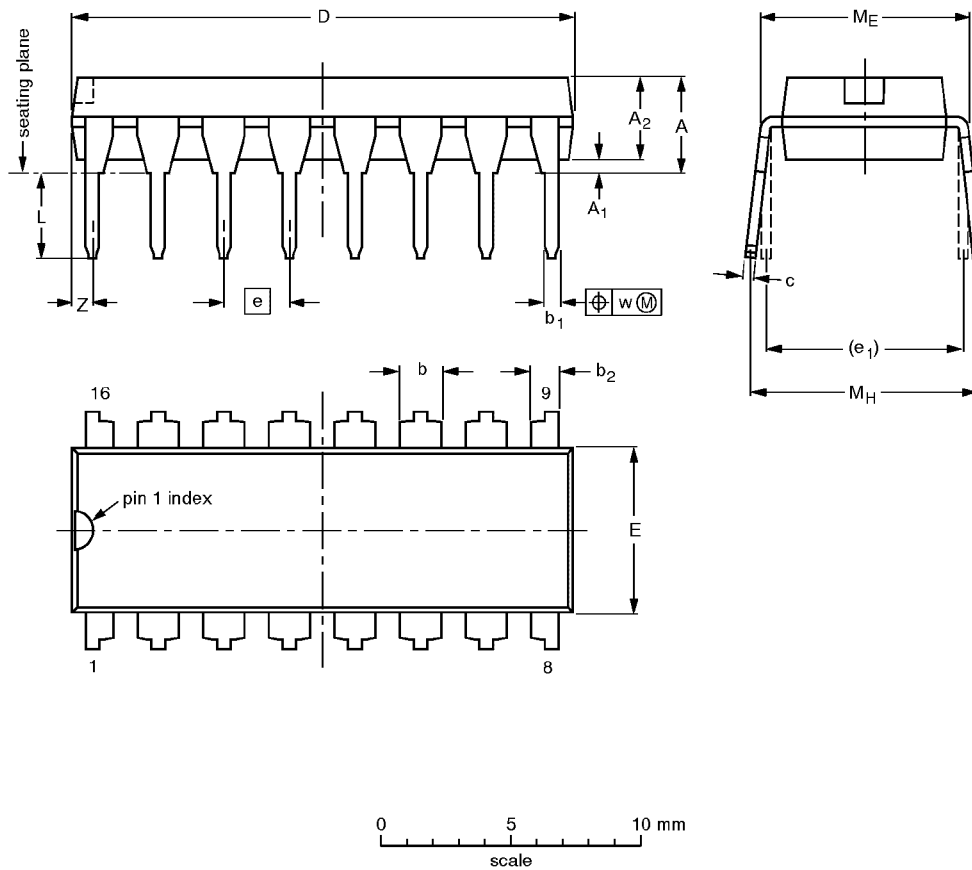
SF00006

Quad D flip-flop

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.030 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | 92-11-17 95-01-14 |

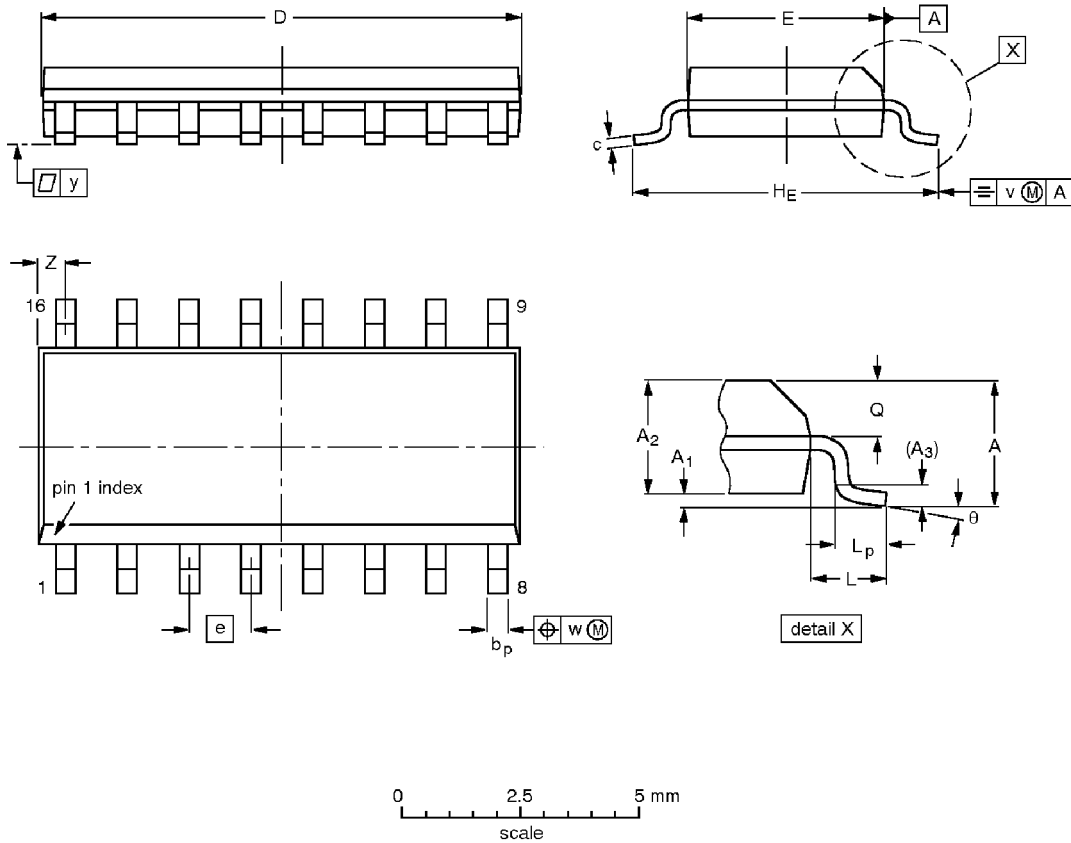
* Discontinued part. Please see the Discontinued Product List.

Quad D flip-flop

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.050 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT109-1 | 076E07S | MS-012AC | | | 95-01-23 97-05-22 |

* Discontinued part. Please see the Discontinued Product List.

Quad D flip-flop

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NOTES

* *Discontinued part. Please see the Discontinued Product List.*

Quad D flip-flop

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397-750-05091

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