

## **MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs**

### **General Description**

The MM54C920/MM74C920, 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, CES and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

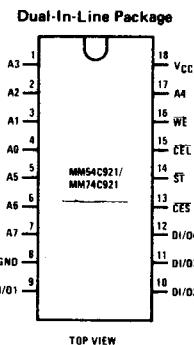
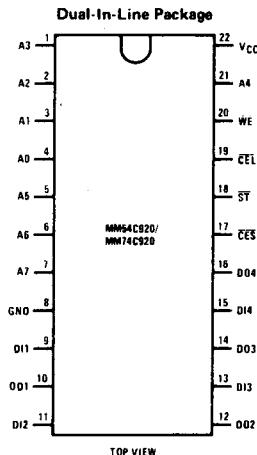
Complete address decoding as well as 2-chip select functions, CEL and CES, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make

these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

### **Features**

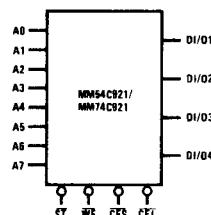
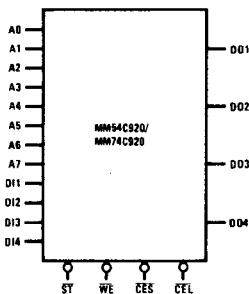
- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C920-3, MM74C921-3
- TRI-STATE® outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V<sub>CC</sub> as low as 2V

### **Connection Diagrams**



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### **Logic Symbols**



## Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in Figure 1. Input addresses and CES are clocked into the input latches by the falling edge of STROBE. Input set-up and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when STROBE rises. The register drives the TRI-STATE® output buffers.

Chip select inputs, CEL and CES, have identical functions except that CES (Chip Enable Stored) is clocked into a latch on the falling edge of STROBE; CEL (Chip Enable Level) is not.

Note that set-up and hold times must be observed on CES. Because CEL is not clocked by STROBE, it may fall after STROBE has fallen without affecting access time provided that the t<sub>OE</sub> requirement is met.

The outputs are in a high impedance state when the chip is not selected (CES or CEL high) or when writing (WE low). Note that the information stored in the output latches will be changed whenever STROBE falls, regardless of the logic states of WE, CEL or CES.

The switching time waveforms in Figures 2, 3 and 4 define the read, write, and output enable/disable parameters respectively.

### Reduced-Voltage Operation

These memories will retain data with reduced V<sub>CC</sub> and hence are useful for battery-backup data storage. Certain precautions must be observed as V<sub>CC</sub> is reduced: (1) input voltages must remain between the V<sub>CC</sub> and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V<sub>CC</sub>, ST logic state must be maintained (either GND or V<sub>CC</sub>) while address control lines stabilize.

### Logic Diagram\*

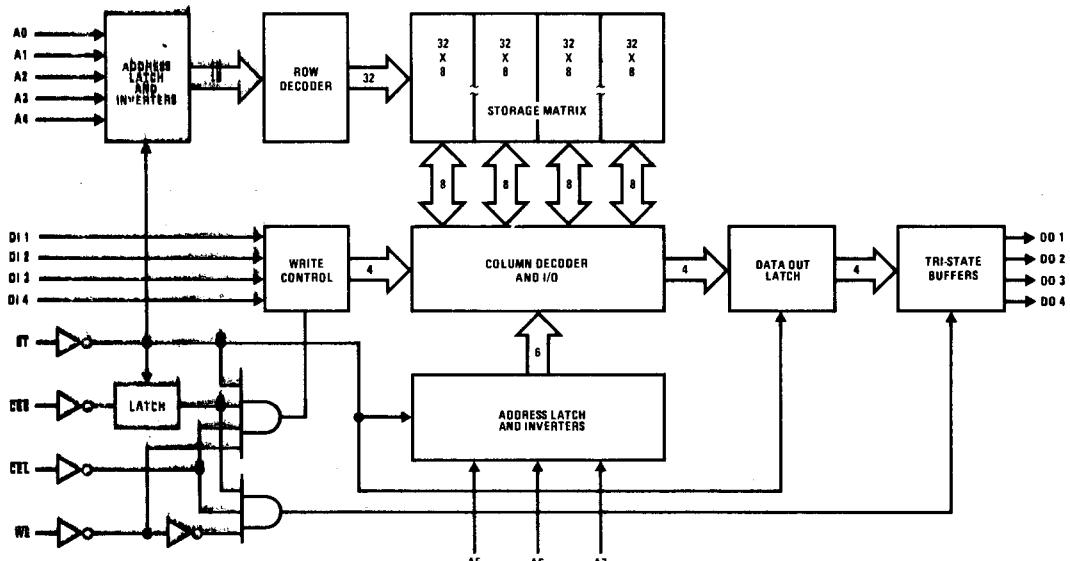


FIGURE 1. MM54C920/MM74C920

\*The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (D1-D4) are connected to data outputs (Q0-Q4).

**Absolute Maximum Ratings** (Note 1)

Supply Voltage, V <sub>CC</sub>	7V
Voltage at Any Pin	-0.3V to V <sub>CC</sub> + 0.3V
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

**Operating Conditions**

	MIN	MAX	UNITS
Supply Voltage (V <sub>CC</sub> )			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T <sub>A</sub> )			
MM54C920, MM54C921	-55	+125	°C
MM74C920, MM74C921	-40	+85	°C
MM74C920-3, MM74C921-3	0	+70	°C

**DC Electrical Characteristics** (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920-3, MM74C921-3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>IH</sub>	Logical "1" Input Voltage		V <sub>CC</sub> -2.0	V <sub>CC</sub>	V <sub>CC</sub> -2.0	V <sub>CC</sub>	V <sub>CC</sub> -1.5	V <sub>CC</sub>	V
V <sub>IL</sub>	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V <sub>OH1</sub>	Logical "1" Output Voltage	I <sub>OH</sub> = -1 mA	2.4		2.4		2.4		V
V <sub>OH2</sub>	Logical "1" Output Voltage	I <sub>OUT</sub> = 0	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V
V <sub>OL1</sub>	Logical "0" Output Voltage	I <sub>OL</sub> = 2 mA		0.4		0.4		0.4	V
V <sub>OL2</sub>	Logical "0" Output Voltage	I <sub>OUT</sub> = 0		0.01		0.01		0.01	V
I <sub>IL</sub>	Input Leakage	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1.0	1.0	-1.0	1.0	-1.0	1.0	μA
I <sub>O</sub>	Output Leakage	0V ≤ V <sub>O</sub> ≤ V <sub>CC</sub> . CEL = V <sub>CC</sub>	-1.0	1.0	-1.0	1.0	-1.0	1.0	μA
I <sub>CC</sub>	Supply Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> , V <sub>O</sub> = 0V		20		10		100	μA
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	(Note 3)	2.0		2.0		2.0		V
I <sub>DR</sub>	I <sub>CC</sub> for Data Retention	CEL = V <sub>CC</sub> = 2V, Typical at 25°C		0.01 (typ)		0.01 (typ)		0.1 (typ)	μA

**Capacitance** (Note 4)

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		4	7	pF
C <sub>O</sub>	Output Capacitance	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		6	9	pF
C <sub>I/O</sub>	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

**Note 1:** "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

**Note 2:** These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

**Note 3:** CEL = V<sub>CC</sub> - 2V or = 2V, whichever is greater.

**Note 4:** Capacitance is guaranteed by periodic testing.

**Truth Table**

<b>ST</b>	<b>CES*</b>	<b>CEL</b>	<b>WE</b>	<b>DI*</b>	<b>FUNCTION</b>
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

\*Set-up and hold times must be met

X = don't care

**AC Electrical Characteristics** (Note 5)

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MM54C920, MM54C921</b>		<b>MM74C920, MM74C921</b>		<b>MM74C920-3 MM74C921-3</b>		<b>UNITS</b>
		<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>	
tC	Cycle Time	290		255		330		ns
tACC	Access Time From Address		275		250		325	ns
tACS	Access Time From Strobe		250		225		300	ns
tAS	Address Set-Up Time	25		25		25		ns
tAH	Address Hold Time	25		25		25		ns
tOE	Output Enable Time		150		130		130	ns
tOD	Output Disable Time		150		130		130	ns
t <sup>ST</sup>	<sup>ST</sup> Pulse Width (Negative)	150		130		165		ns
t <sup>ST</sup>	<sup>ST</sup> Pulse Width (Positive)	140		125		165		ns
tWP	Write Pulse Width (Negative)	150		130		165		ns
tDS	Data Set-Up Time	100		90		90		ns
tDH	Data Hold Time	60		60		60		ns

**Note 5:** These limits apply over the operating range specified in the "Operating Conditions" with t<sub>RISE</sub> = t<sub>FALL</sub> = 5 ns, load = 1 TTL gate + 50 pF.

## Switching Time Waveforms

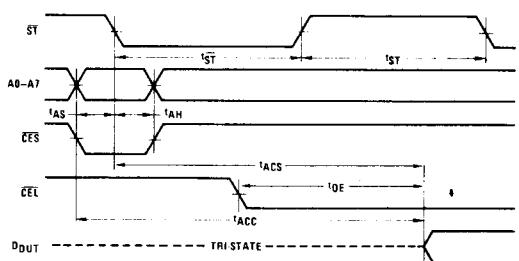
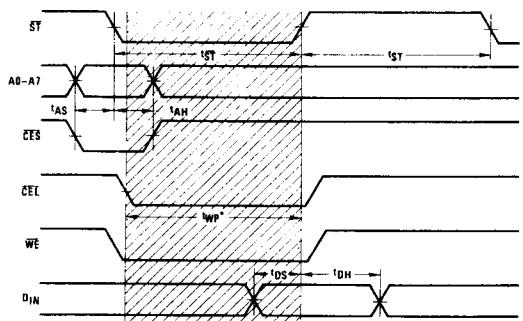


FIGURE 2. Read Cycle ( $\overline{WE} = V_{IH}$ )



\*  $t_{WP}$  (the Write Pulse Width) is the time  $\overline{ST}$ ,  $\overline{CEL}$  and  $\overline{WE}$  are coincidentally low

FIGURE 3. Write Cycle

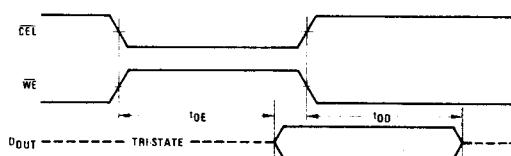
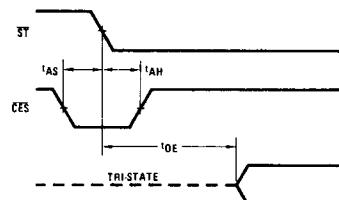
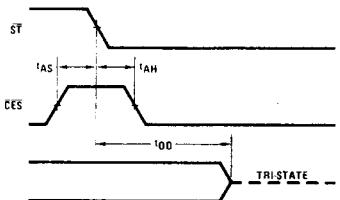
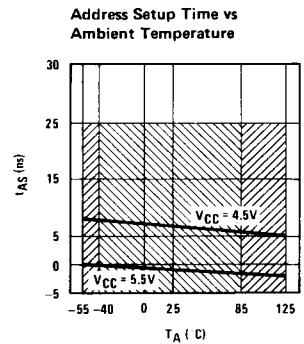
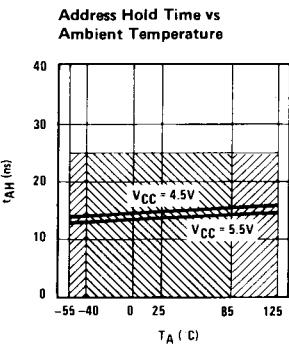
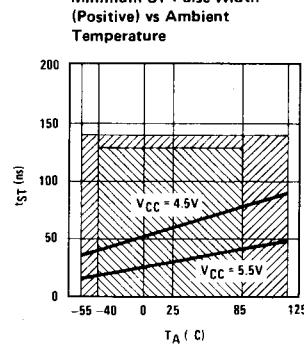
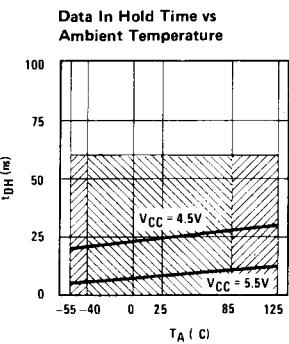
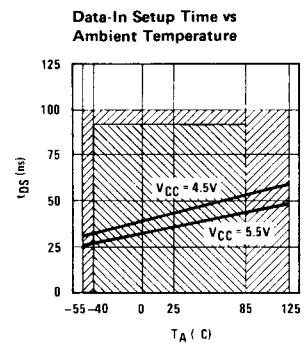
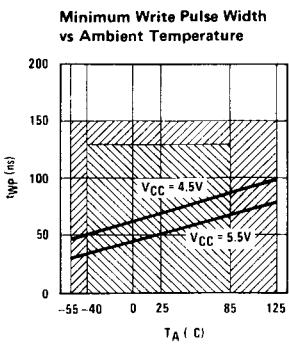
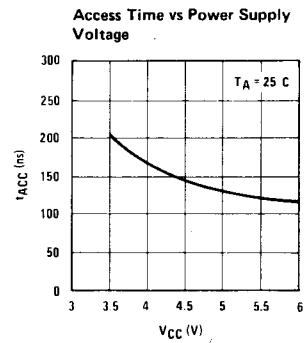
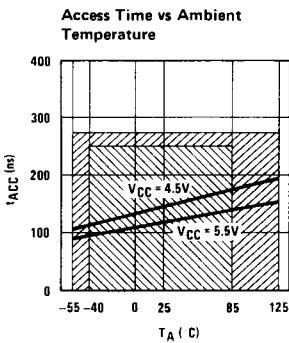


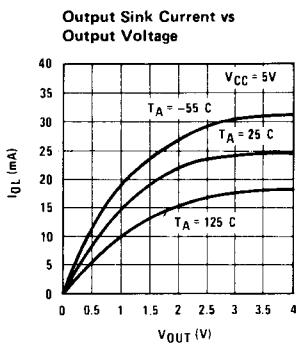
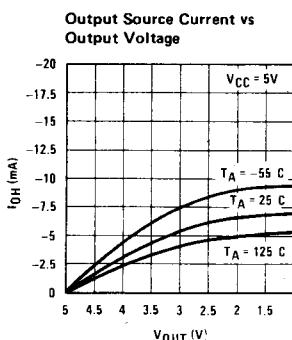
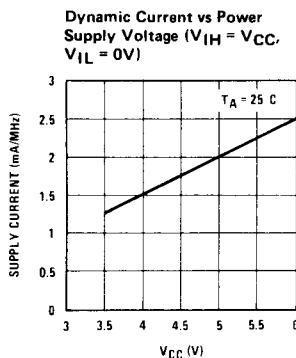
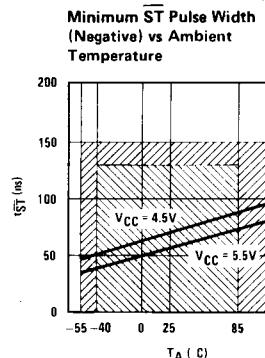
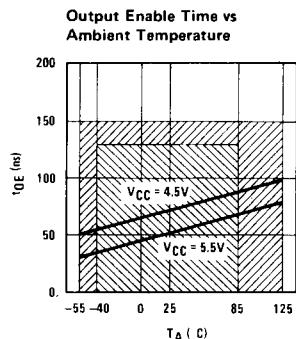
FIGURE 4. Output Enable/Disable

# Typical Performance Characteristics



# Typical Performance Characteristics (Continued)

**MM54C920/MM74C920, MM54C921/MM74C921**



Test Limit MM54C920, MM54C921



Test Limit MM74C920, MM74C921

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