

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT86**

### Quad 2-input EXCLUSIVE-OR gate

Product specification  
File under Integrated Circuits, IC06

December 1990

**Quad 2-input EXCLUSIVE-OR gate****74HC/HCT86****FEATURES**

- Output capability: standard
- I<sub>CC</sub> category: SSI

**GENERAL DESCRIPTION**

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT86 provide the EXCLUSIVE-OR function.

**QUICK REFERENCE DATA**

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	11	14	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION**

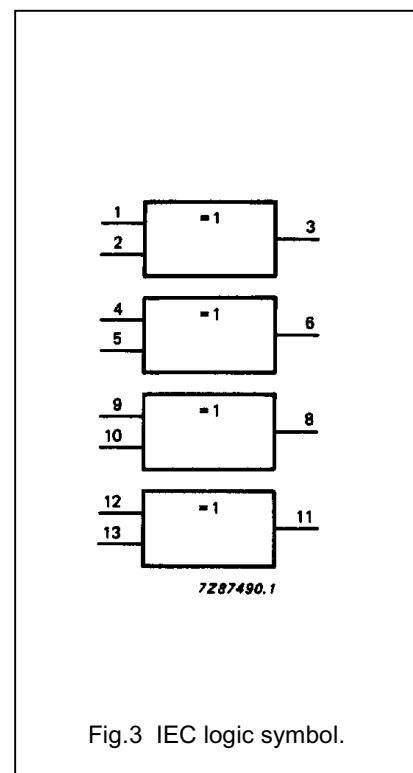
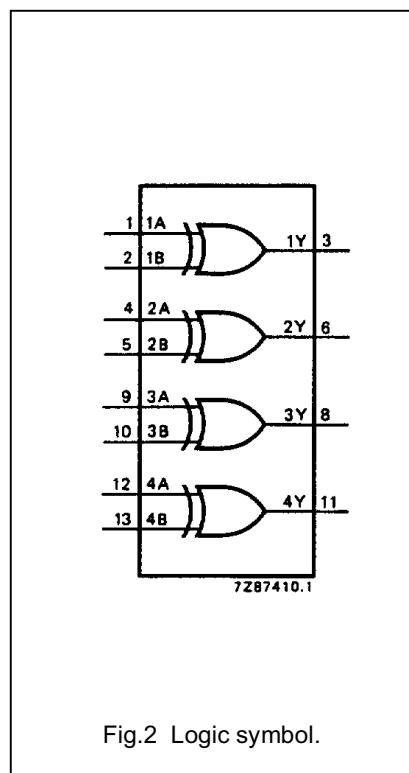
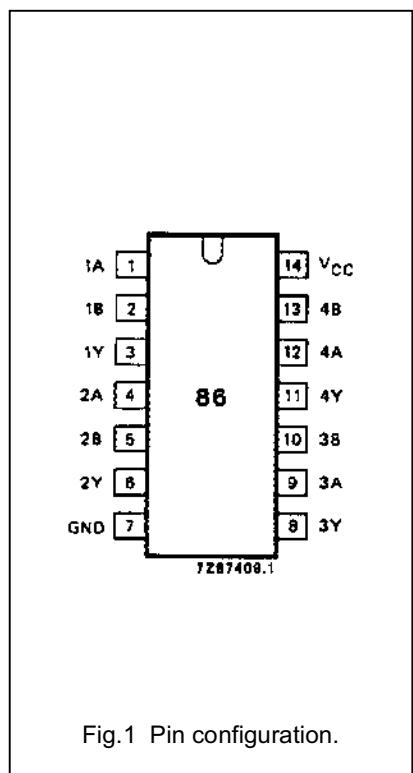
See "74HC/HCT/HCU/HCMOS Logic Package Information".

## Quad 2-input EXCLUSIVE-OR gate

74HC/HCT86

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



## Quad 2-input EXCLUSIVE-OR gate

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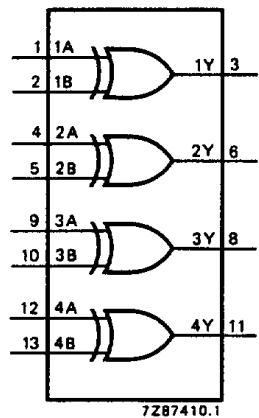


Fig.4 Functional diagram.

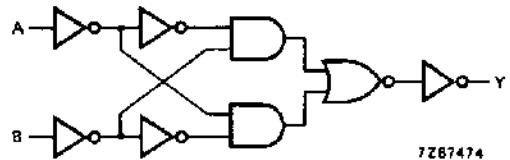


Fig.5 Logic diagram (one gate).

## FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

## Notes

1. H = HIGH voltage level  
L = LOW voltage level

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

 $I_{CC}$  category: SSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>TPLH</sub>	propagation delay nA, nB to nY		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6	

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

 $I_{CC}$  category: SSI

## Notes to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.  
 To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

## AC CHARACTERISTICS FOR 74HCT

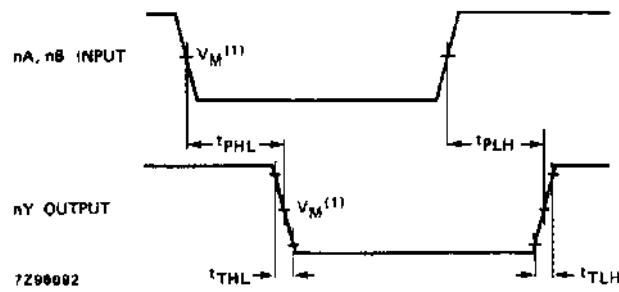
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>TPLH</sub>	propagation delay nA, nB to nY		17	32		40		48	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6	

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## AC WAVEFORMS



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".