DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications

74HC/HCT4066
Quad bilateral switches

Product specification
Supersedes data of 1998 Oct 02
File under Integrated Circuits, IC06

1998 Nov 10

Philips
Semiconductors

PHILIPS

FEATURES

- Very low "ON" resistance:
  50 Ω (typ.) at V_{CC} = 4.5 V
  45 Ω (typ.) at V_{CC} = 6.0 V
  35 Ω (typ.) at V_{CC} = 9.0 V
- Output capability: non-standard
- I_{CC} category: SSI.

GENERAL DESCRIPTION

The 74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4066" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4066 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The "4066" is pin compatible with the "4016" but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn-on time nE to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	11	12	ns
t_{PHZ}/ t_{PLZ}	turn-off time nE to V_{os}		13	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	11	12	pF
C_S	max. switch capacitance		8	8	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   a) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   b) f_i = input frequency in MHz
   c) f_o = output frequency in MHz
   d) $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
   e) C_L = output load capacitance in pF
   f) C_S = maximum switch capacitance in pF
   g) V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
74HC4066	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC4066	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC4066	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC4066	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT4066	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT4066	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT4066	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT4066	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
7	GND	ground (0 V)
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

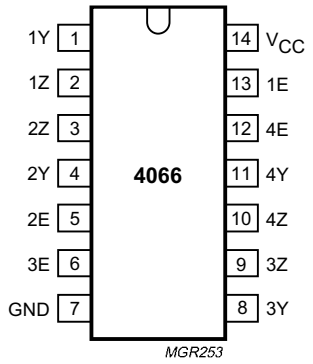


Fig.1 Pin configuration.

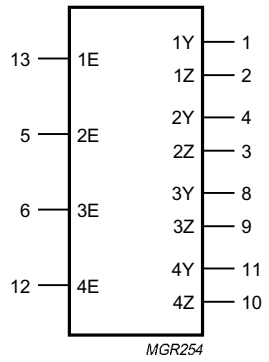


Fig.2 Logic symbol.

a. b.

Fig.3 IEC logic symbol.

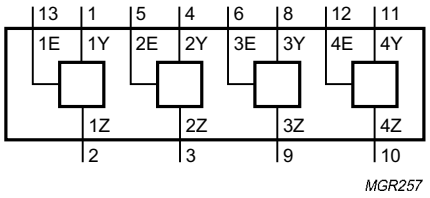


Fig.4 Functional diagram.

FUNCTION TABLE

INPUT NE	SWITCH
L	off
H	on

Note

1. H = HIGH voltage level; L = LOW voltage level.

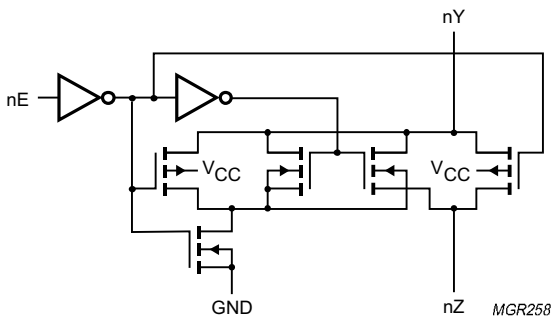


Fig.5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134) Voltages are referenced to GND (GND = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_{IS}$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: –40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note

1. To avoid drawing V_{CC} current out of terminal nZ, when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	–40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	–40		+125	–40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000		6.0	500	ns	V_{CC} = 2.0 V
				500					V_{CC} = 4.5 V
				400					V_{CC} = 6.0 V
				250					V_{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V; For 74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT											
		+25			−40 to +85		−40 to +125			V_{CC} (V)	I_S (μA)	V_{IS}	V_I
		min.	typ.	max.	min.	max.	min.	max.					
R_{ON}	ON-resistance (peak)		–	–		–		–	Ω	2.0	100	V_{CC} to GND	V_{IH} or V_{IL}
			54	95		118		142	Ω	4.5	1000		
			42	84		105		126	Ω	6.0	1000		
			32	70		88		105	Ω	9.0	1000		
R_{ON}	ON-resistance (rail)		80	–		–		–	Ω	2.0	100	GND	V_{IH} or V_{IL}
			35	75		95		115	Ω	4.5	1000		
			27	65		82		100	Ω	6.0	1000		
			20	55		70		85	Ω	9.0	1000		
R_{ON}	ON-resistance (rail)		100	–		–		–	Ω	2.0	100	V_{CC}	V_{IH} or V_{IL}
			42	80		106		128	Ω	4.5	1000		
			35	75		94		113	Ω	6.0	1000		
			27	60		78		95	Ω	9.0	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels		–						Ω	2.0		V_{CC} to GND	V_{IH} or V_{IL}
			5						Ω	4.5			
			4						Ω	6.0			
			3						Ω	9.0			

Note

1. At supply voltages approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

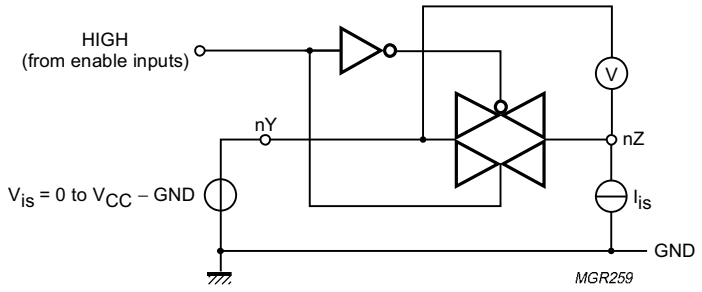


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

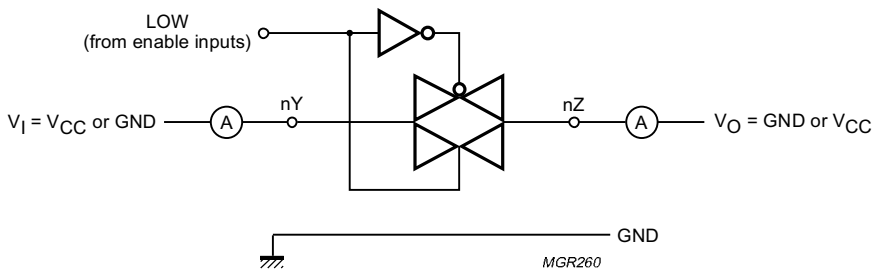


Fig.7 Test circuit for measuring OFF-state current.

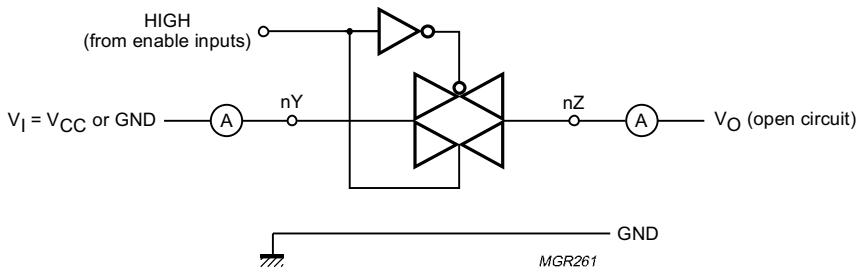


Fig.8 Test circuit for measuring ON-state current.

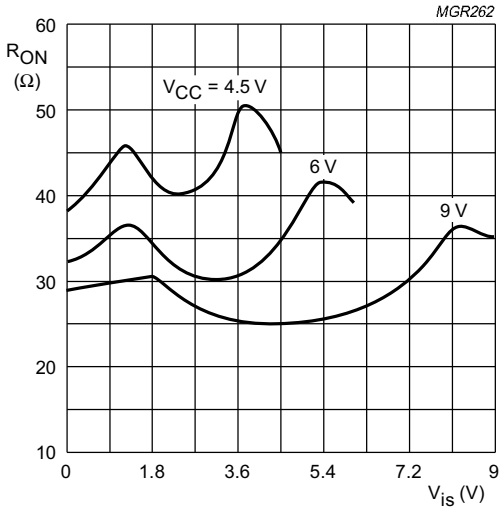


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}.

DC CHARACTERISTICS FOR 74HC

Voltage are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max				
V_{IH}	HIGH-level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		
V_{IL}	LOW-level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$V_S = V_{CC} - GND$ (see Fig.7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	V_{IH} or V_{IL}	$V_S = V_{CC} - GND$ (see Fig.8)
I_{CC}	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μA	6.0 10.0	V_{CC} or GND	V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		8	60		75		90	ns	2.0	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)
			3	12		15		18		4.5	
			2	10		13		15		6.0	
			2	8		10		12		9.0	
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}		36	100		125		150	ns	2.0	$R_L = 1$ kΩ; $C_L = 50$ pF (see Figs 19 and 20)
			13	20		25		30		4.5	
			10	17		21		26		6.0	
			8	13		16		20		9.0	
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}		44	150		190		225	ns	2.0	$R_L = 1$ kΩ; $C_L = 50$ pF (see Figs 19 and 20)
			16	30		38		45		4.5	
			13	26		33		38		6.0	
			16	24		16		20		9.0	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH-level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW-level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$V_S = V_{CC} - GND$ (see Fig.7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$V_S = V_{CC} - GND$ (see Fig.8)
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	4.5 to 5.5	V_{CC} or GND	V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} − 2.1 V	other inputs at V_{CC} or GND

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

Table 1

INPUT	UNIT LOAD COEFFICIENT
nE	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		3	12		15		18	ns	4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}		12	24		30		36	ns	4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Figs 19 and 20)
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}		20	35		44		53	ns	4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Figs 19 and 20)

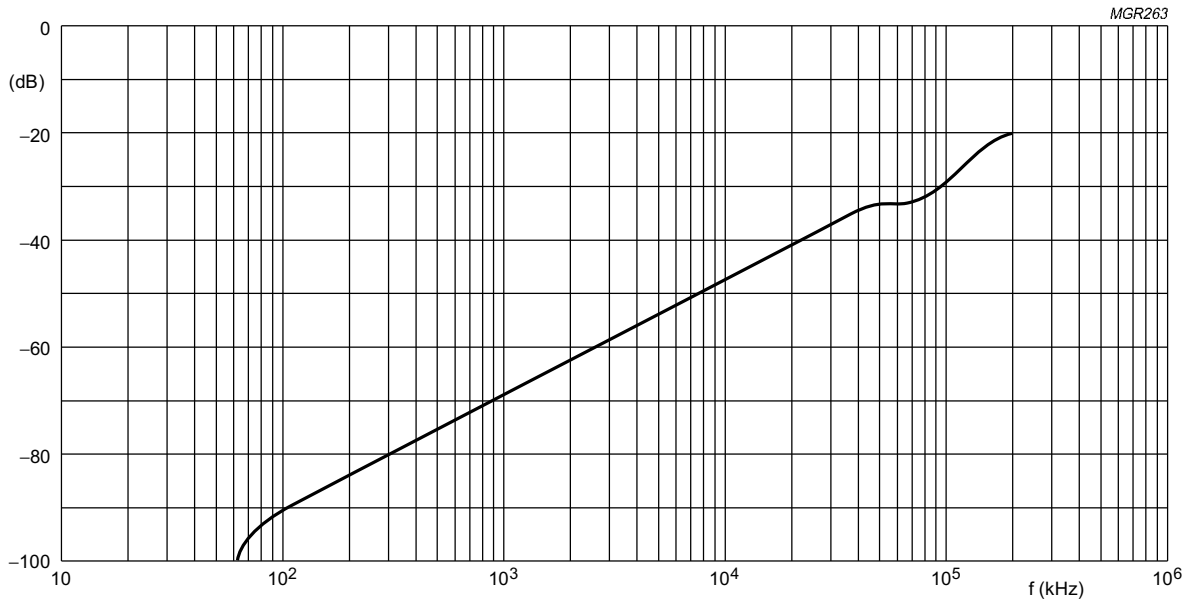
ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{IS(p-p)}$ (V)	CONDITIONS
	sine wave distortion f = 1 kHz	0.04 0.02	% %	4.5 9.0	4.0 8.0	$R_L = 10$ kΩ; $C_L = 50$ pF (see Fig.16)
	sine wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	$R_L = 10$ kΩ; $C_L = 50$ pF (see Fig.16)
	switch “OFF” signal feed-through	−50 −50	dB dB	4.5 9.0	note 3	$R_L = 600$ Ω; $C_L = 50$ pF; f = 1 MHz (see Figs 10 and 17)
	crosstalk between any two switches	−60 −60	dB dB	4.5 9.0	note 3	$R_L = 600$ Ω; $C_L = 50$ pF; f = 1 MHz (see Fig.12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		$R_L = 600$ Ω; $C_L = 50$ pF; f = 1 MHz (nE, square wave between V_{CC} and GND, $t_r = t_f = 6$ ns) (see Fig.14)
f_{max}	minimum frequency response (−3 dB)	180 200	MHz MHz	4.5 9.0	note 4	$R_L = 50$ Ω; $C_L = 10$ pF (see Figs 11 and 15)
C_S	maximum switch capacitance	8	pF			

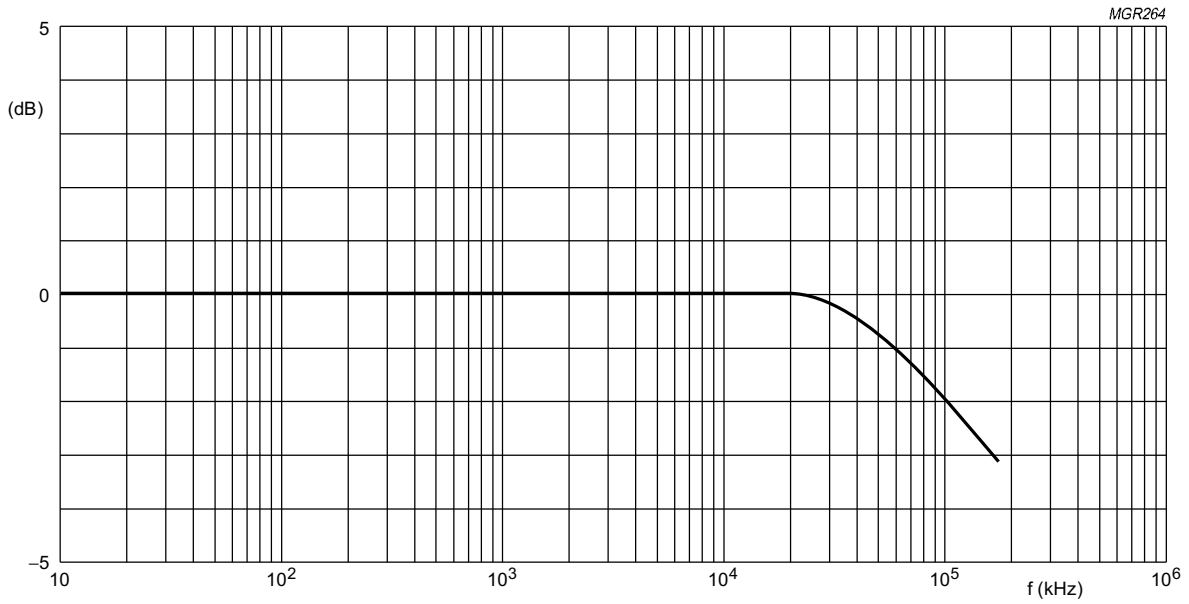
Notes

1. V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
2. V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.
3. Adjust input voltage V_{is} is 0 dBM level (0 dBM = 1 mW into 600 Ω).
4. Adjust input voltage V_{is} is 0 dBM level at V_{os} for 1 MHz (0 dBM = 1 mW into 50 Ω).



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.10 Typical switch “OFF” signal feed-through as a function of frequency.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.11 Typical frequency response.

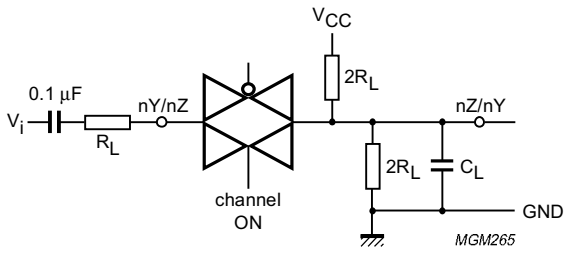


Fig.12 Test circuit for measuring crosstalk between any two switches; channel ON condition.

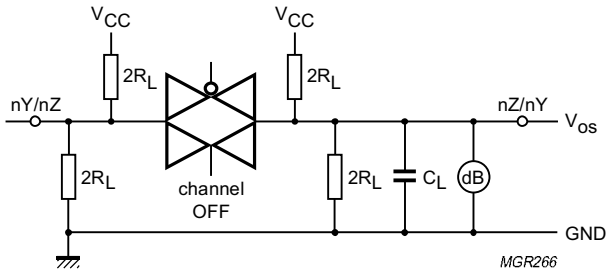


Fig.13 Test circuit for measuring crosstalk between any two switches; channel OFF condition.

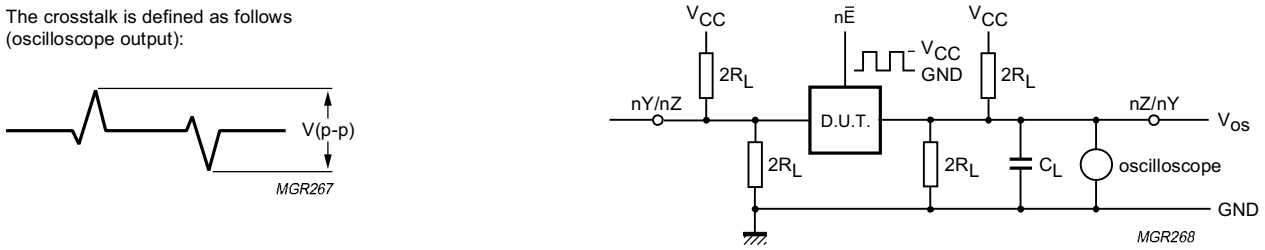
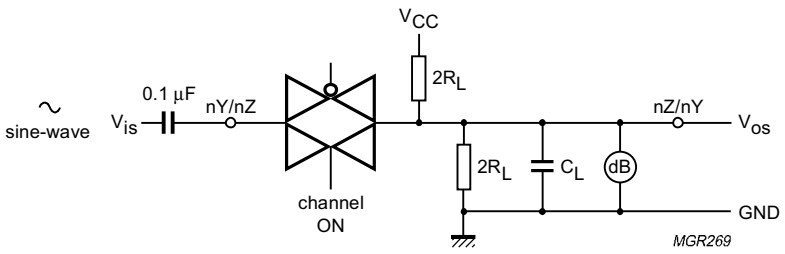


Fig.14 Test circuit for measuring crosstalk between control and any switch.



Adjust input voltage to obtain 0 dBM at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{os}.

Fig.15 Test circuit for measuring minimum frequency response.

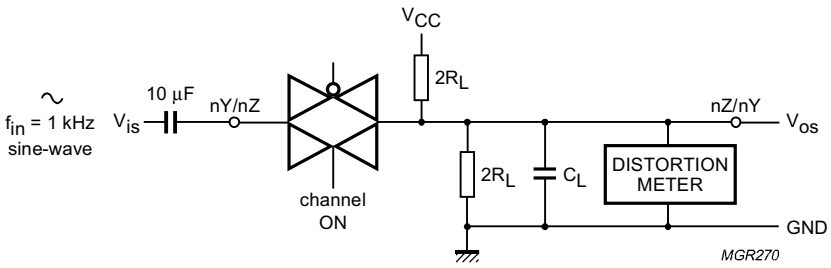


Fig.16 Test circuit for measuring sine wave distortion.

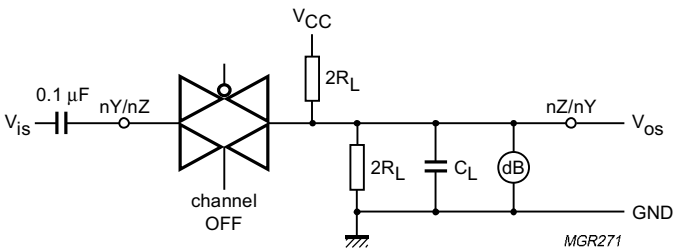
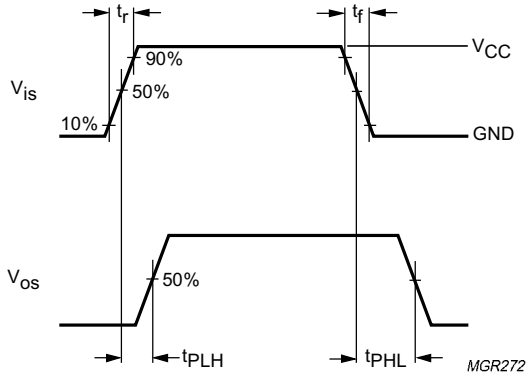


Fig.17 Test circuit for measuring switch “OFF” signal feed-through.

AC WAVEFORMS



(1) HC: V_M = 50%; V_I = GND to V_{CC}; HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

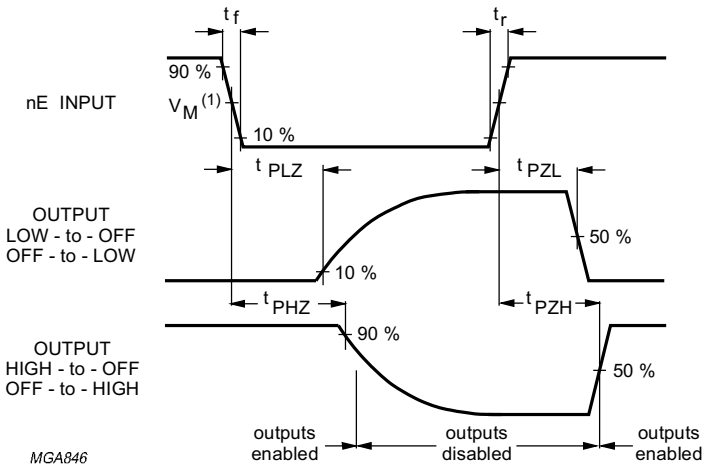


Fig.19 Waveforms showing the turn-on and turn-off times.

TEST CIRCUIT AND WAVEFORMS

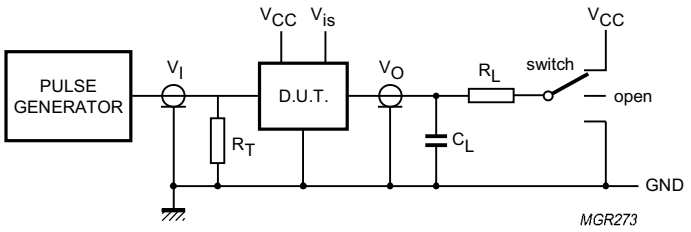


Fig.20 Test circuit for measuring AC performance.

Table 2 Conditions

TEST	SWITCH	V_{IS}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
others	open	pulse

Table 3 Definitions for Figs 20 and 21:

SYMBOL	DEFINITION
C_L	load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values)
R_T	termination resistance should be equal to the output impedance Z_O of the pulse generator
t_r	t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor

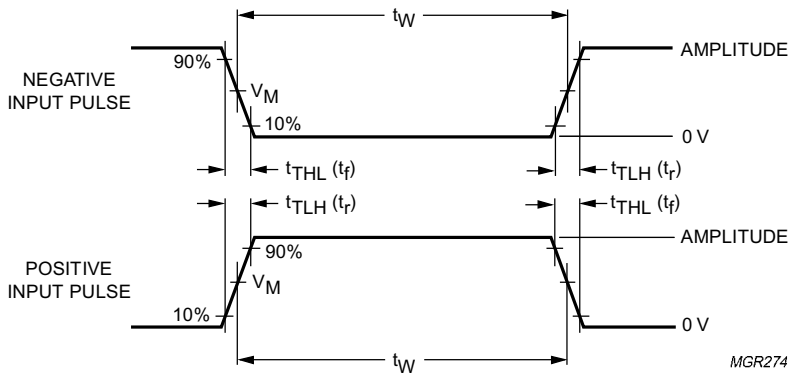


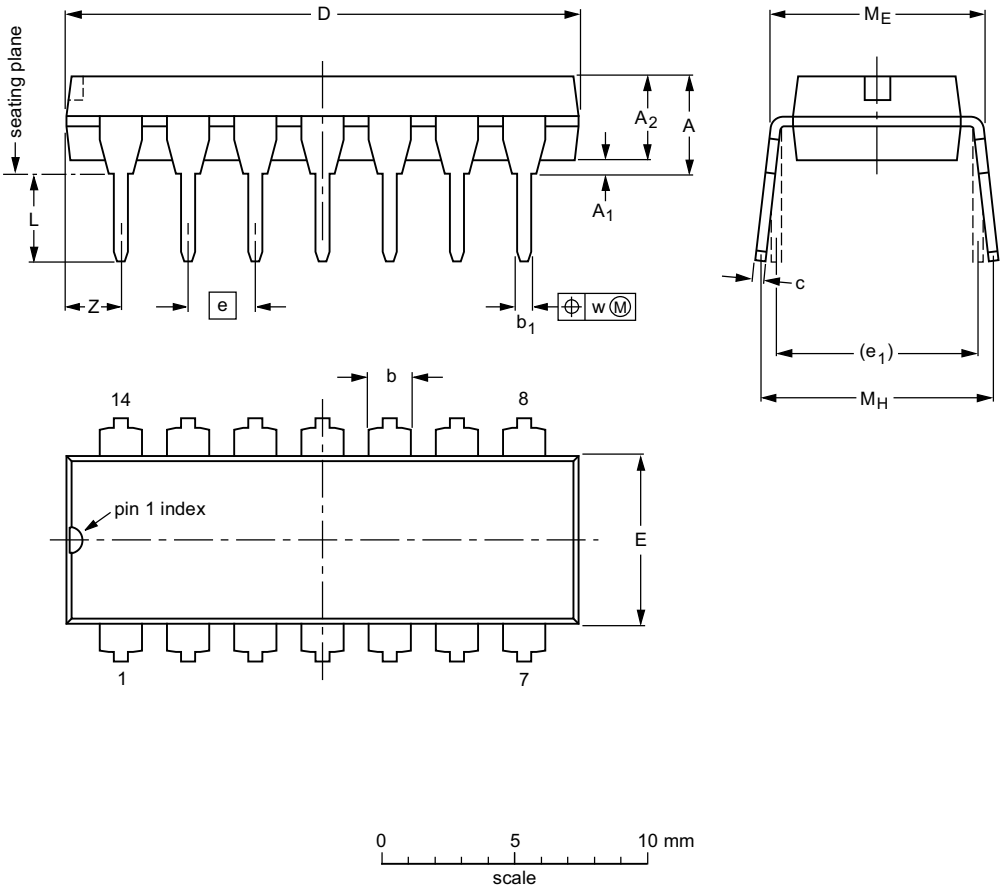
Fig.21 Input pulse definitions.

Table 4

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

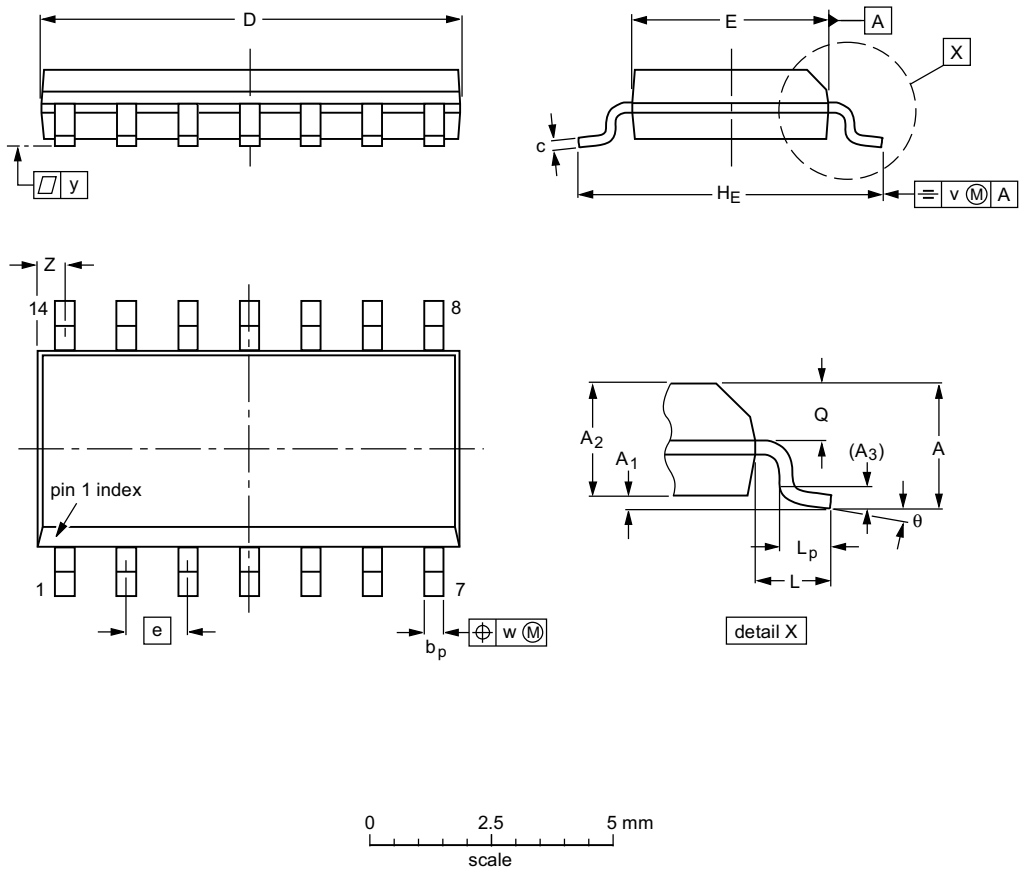
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

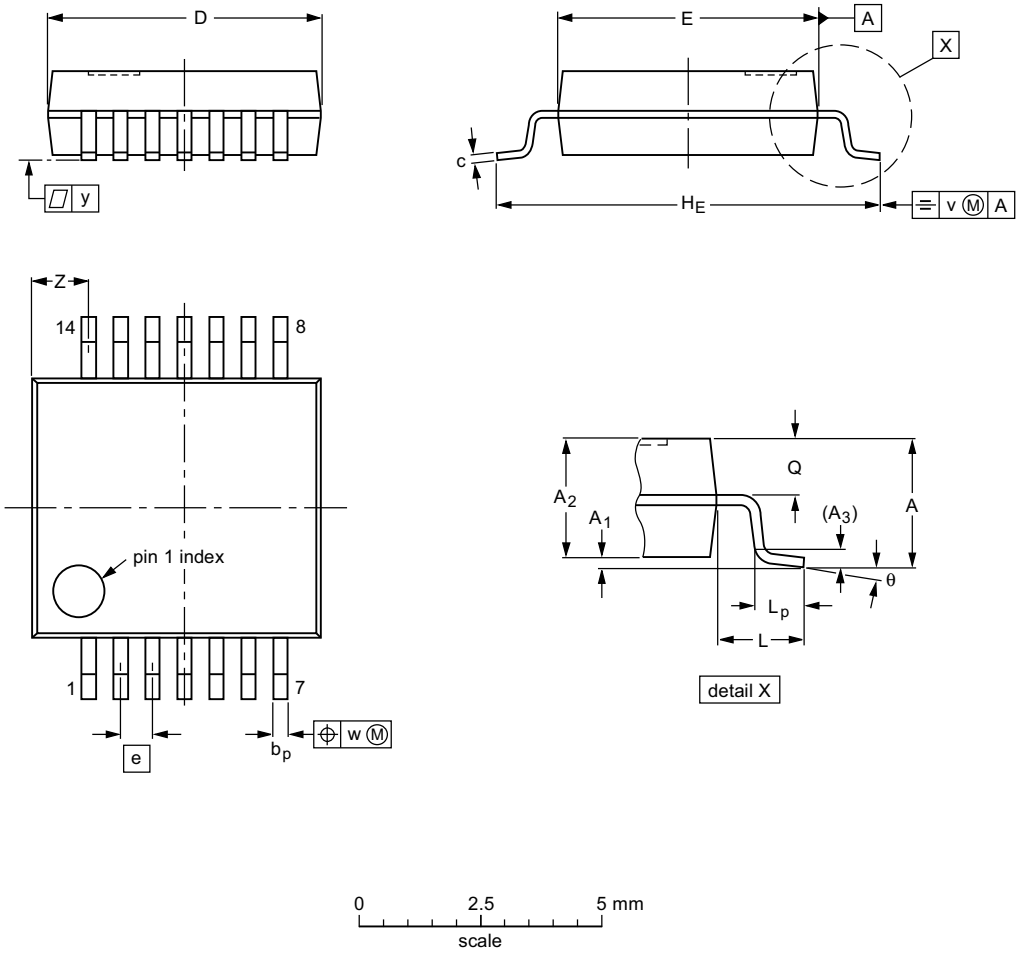
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

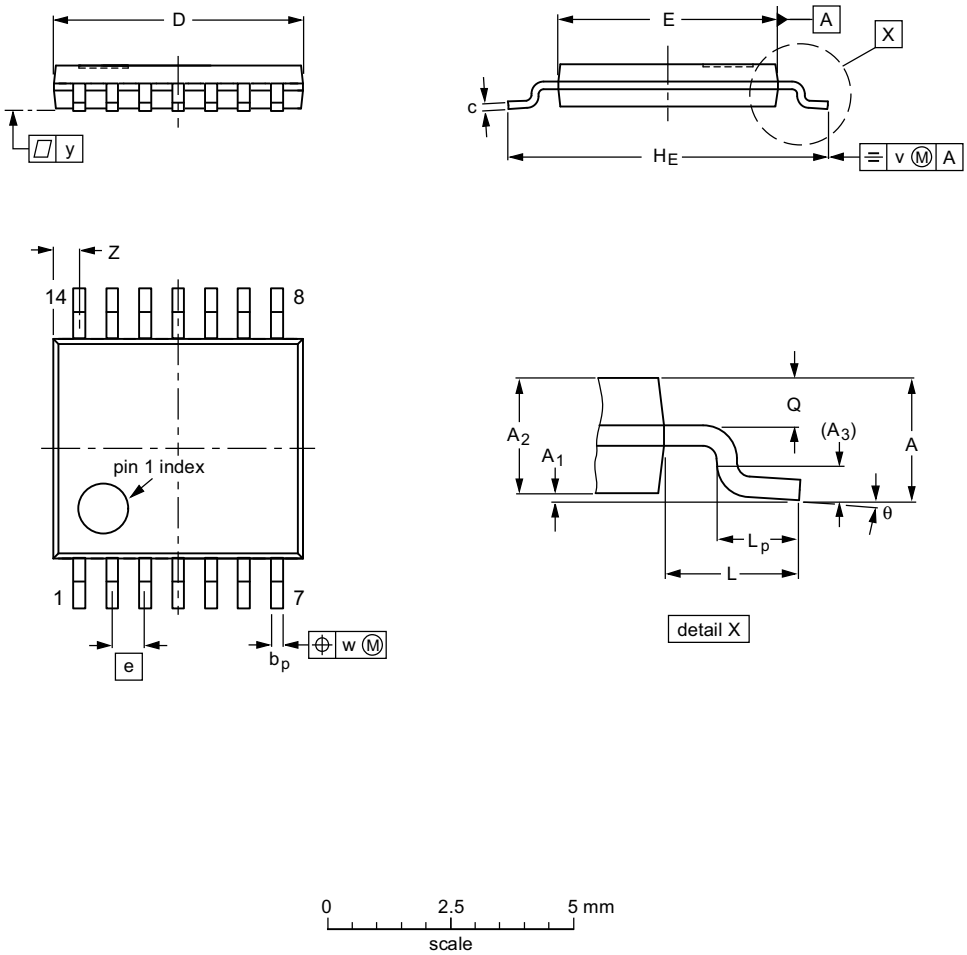
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	HLQFP, HSQFP, HSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SQFP	not suitable	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Product specification	This data sheet contains final product specifications.
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Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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