

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT4020**

### **14-stage binary ripple counter**

Product specification  
File under Integrated Circuits, IC06

September 1993

## 14-stage binary ripple counter

## 74HC/HCT4020

## FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q<sub>0</sub>, Q<sub>3</sub> to Q<sub>13</sub>).

The counter is advanced on the HIGH-to-LOW transition of  $\overline{CP}$ .

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ .

Each counter stage is a static toggle flip-flop.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	$\overline{CP}$ to Q <sub>0</sub>		11	15	ns
	Q <sub>n</sub> to Q <sub>n+1</sub>		6	6	ns
	MR to Q <sub>n</sub>		17	19	ns
f <sub>max</sub>	maximum clock frequency		101	52	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	19	20	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

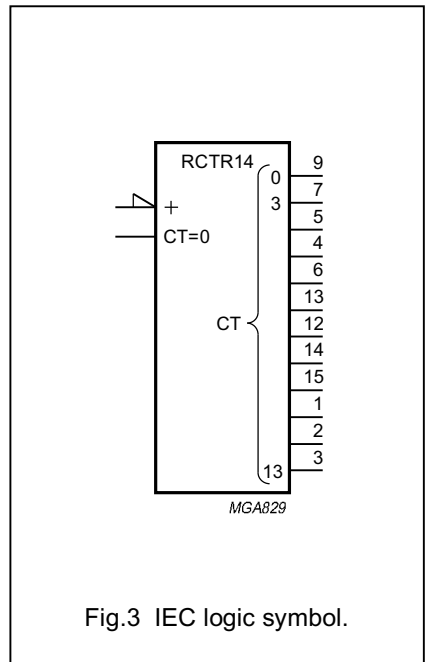
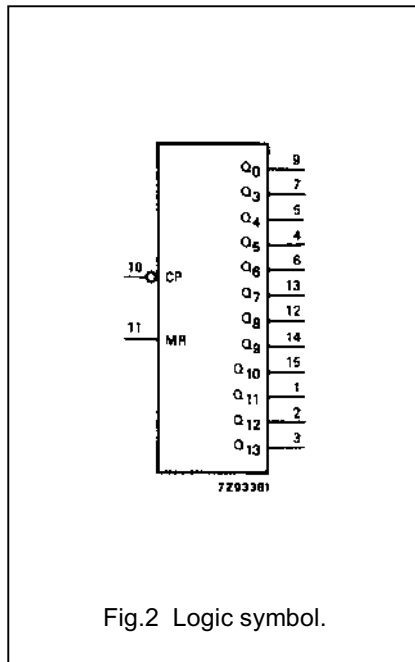
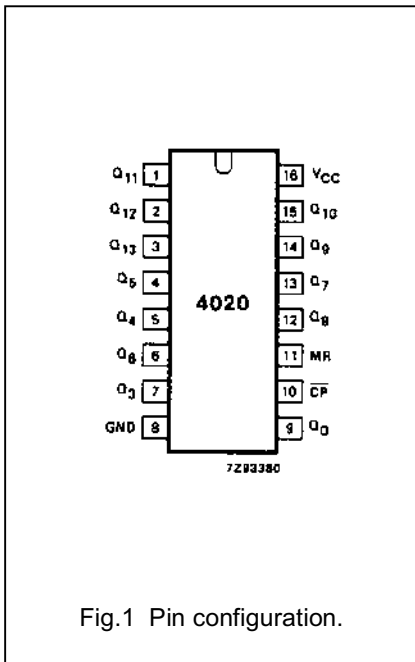
See "74HC/HCT/HCU/HCMOS Logic Package Information".

14-stage binary ripple counter

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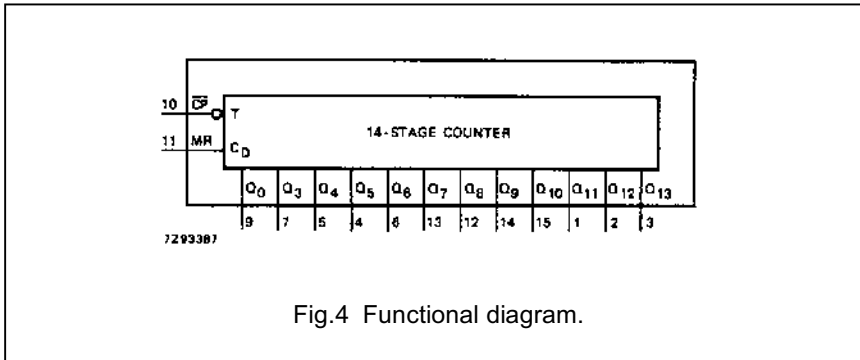
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q <sub>0</sub> , Q <sub>3</sub> to Q <sub>13</sub>	parallel outputs
8	GND	ground (0 V)
10	$\overline{\text{CP}}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V <sub>CC</sub>	positive supply voltage



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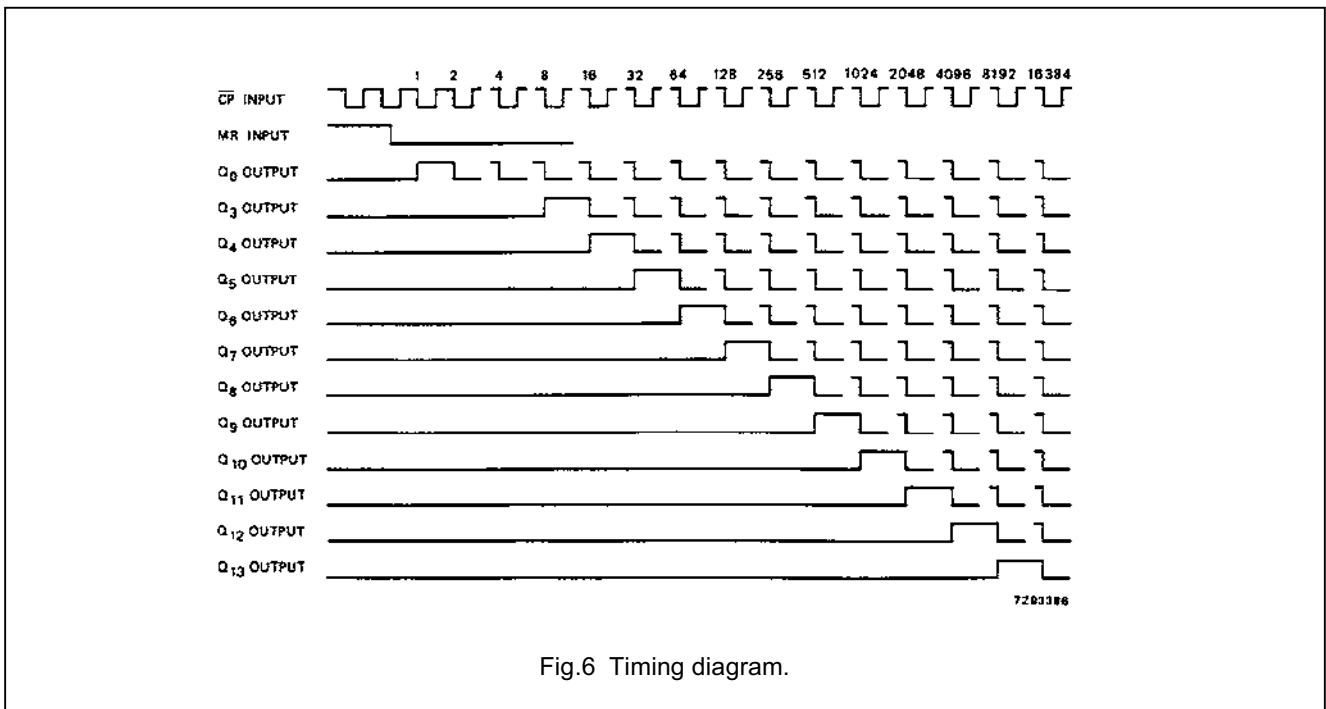
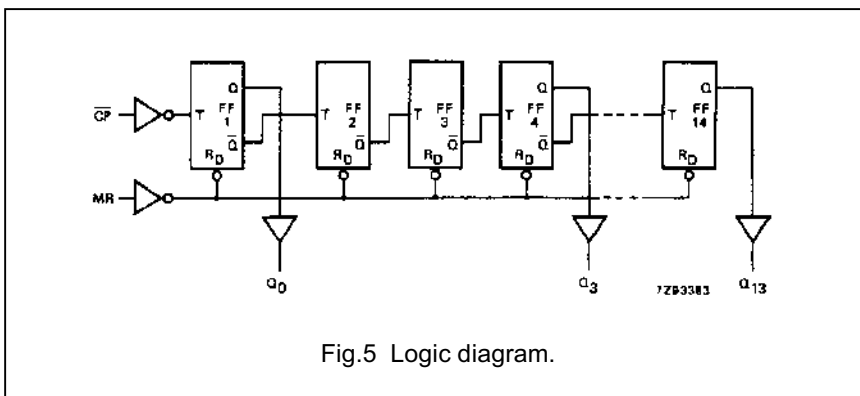


### FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	$Q_0, Q_3$ to $Q_{13}$
↑	L	no change
↓	L	count
X	H	L

### Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH clock transition  
↓ = HIGH-to-LOW clock transition



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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		22 8 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		55 20 16	170 34 29		215 43 37		225 51 43	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>rem</sub>	removal time MR to CP	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	30 92 109		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

**AC CHARACTERISTICS FOR 74HCT**

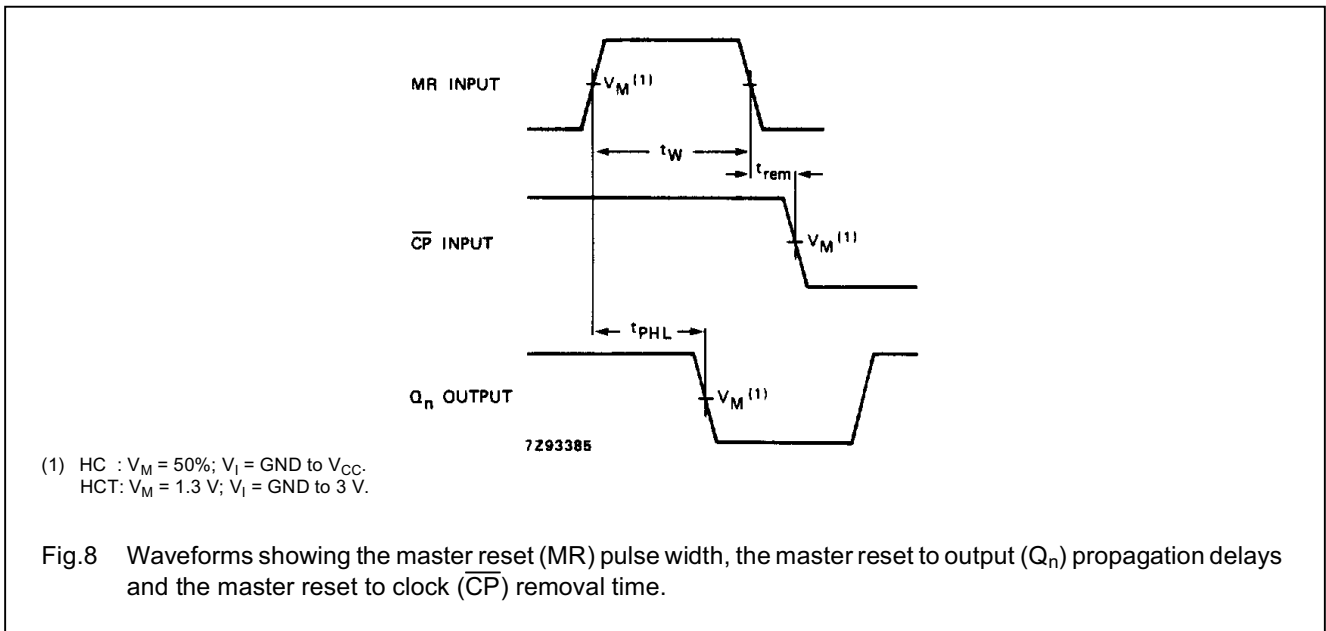
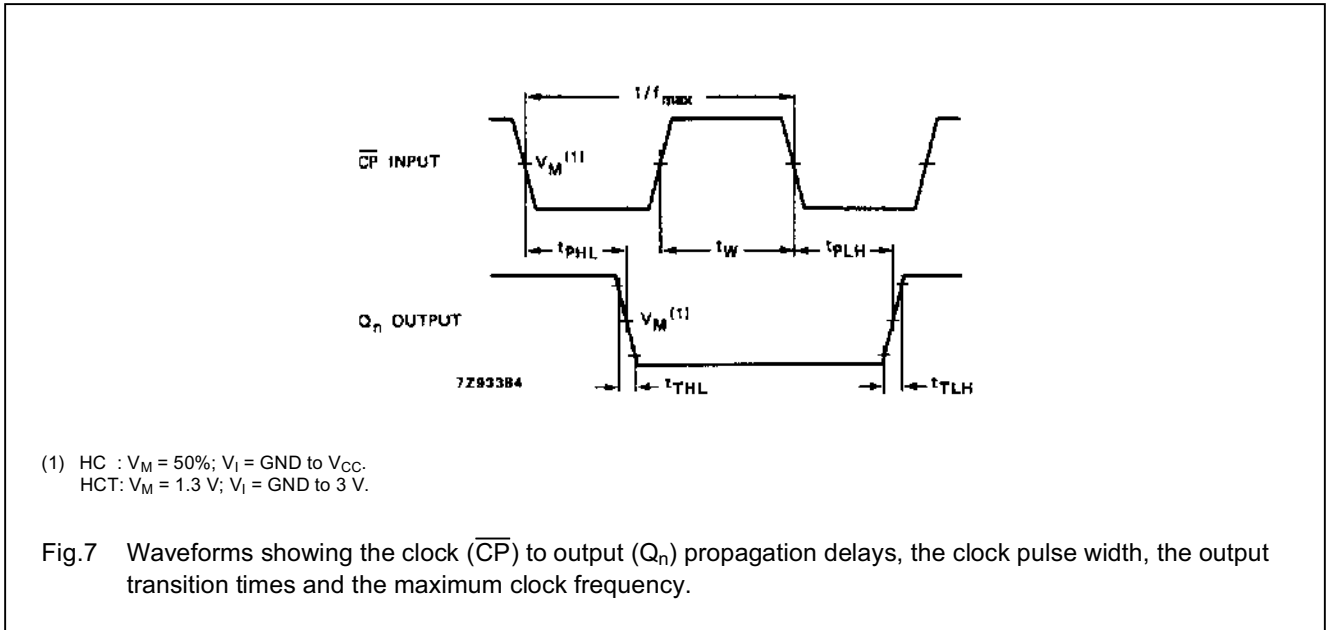
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		18	36		45		54	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		8	15		19		22	ns	4.5	Fig.7	
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		22	45		56		68	ns	4.5	Fig.8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.7	
t <sub>W</sub>	clock pulse width HIGH or LOW	20	7		25		30		ns	4.5	Fig.7	
t <sub>W</sub>	master reset pulse width HIGH	20	8		25		30		ns	4.5	Fig.8	
t <sub>rem</sub>	removal time MR to CP	10	2		13		15		ns	4.5	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	25	47		20		17		MHz	4.5	Fig.7	

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".