

# DATA SHEET

~~74F398\*~~, **74F399**

**Registers**

\* Discontinued part. Please see the Discontinued Product List.

Product specification  
Supersedes data of 1990 Apr 08  
IC15 Data Handbook

1999 Jan 08

## Registers

## 74F398\*, 74F399

74F398 Quad 2-Port Register with True and Complementary Outputs  
74F399 Quad 2-Port Register

## FEATURES

- Select inputs from two data sources
- Fully positive edge-triggered
- Both True and Complementary outputs—74F398

## DESCRIPTION

The 74F398 and 74F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

The 74F399 is the 16-pin version of the 74F398, with only the true (Qn) outputs of the flip-flops available.

The 74F398 and 74F399 are high speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I0n, I1n) and Select input (S) must be stable only a setup time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 74F398 has both Q and  $\bar{Q}$  outputs.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
16-pin plastic DIP	N74F399N	SOT38-4
16-pin plastic SO	N74F399D	SOT109-1

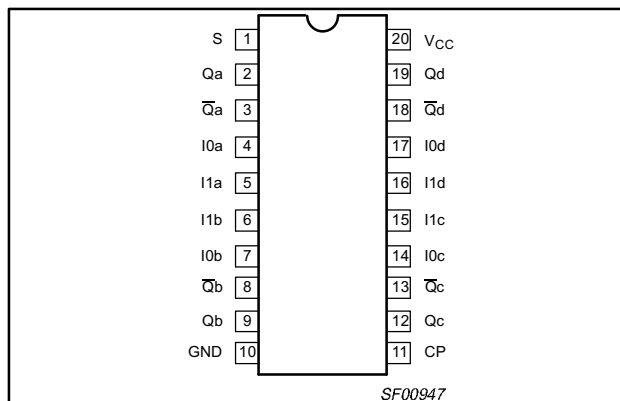
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0a, I0b, I0c, I0d	Data inputs from source 0	1.0/1.0	20 $\mu$ A/0.6mA
I1a, I1b, I1c, I1d	Data inputs from source 1	1.0/1.0	20 $\mu$ A/0.6mA
S	Common Select input	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
Qa, Qb, Qc, Qd	Register true outputs	50/33	1.0mA/20mA
$\bar{Q}a, \bar{Q}b, \bar{Q}c, \bar{Q}d$	Register complementary outputs (74F398)	50/33	1.0mA/20mA

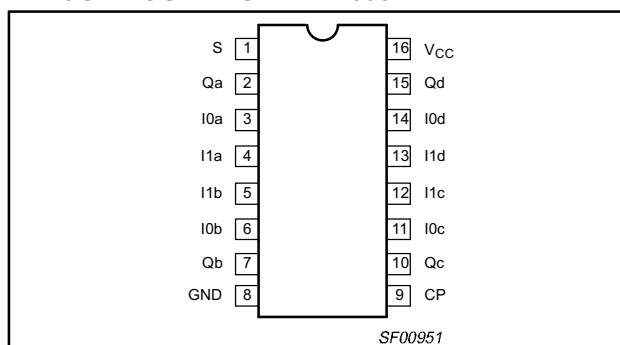
## NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## PIN CONFIGURATION – 74F398



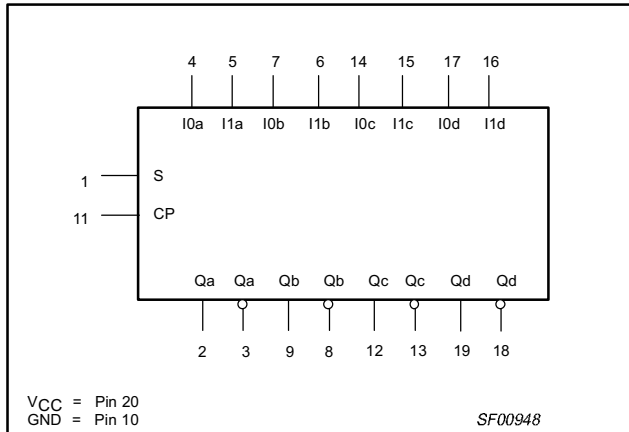
## PIN CONFIGURATION – 74F399



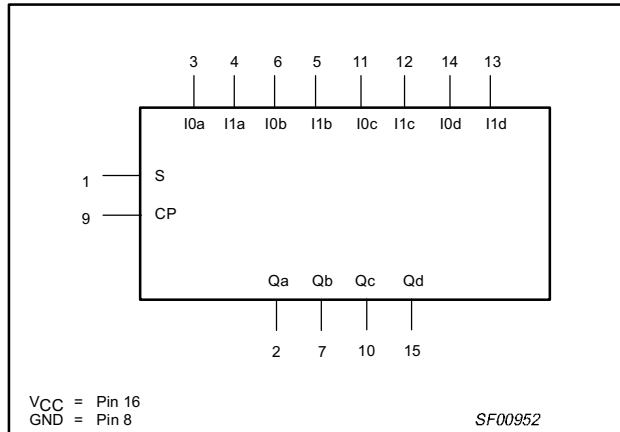
# Registers

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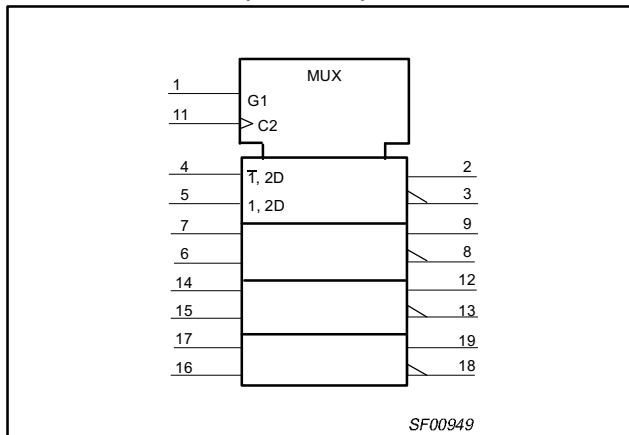
## LOGIC SYMBOL – 74F398



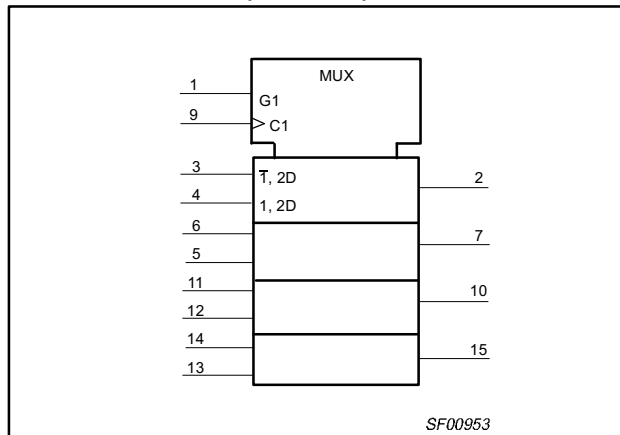
## LOGIC SYMBOL – 74F399



## IEC/IEEE SYMBOL (IEEE/IEC) – 74F398



## IEC/IEEE SYMBOL (IEEE/IEC) – 74F399



## FUNCTION TABLE

INPUTS				OUTPUTS	
CP	S	I0n	I1n	Qn	$\bar{Q}n$ (74F398 only)
↑	l	l	X	L	H
↑	l	h	X	H	L
↑	h	X	l	L	H
↑	h	X	h	H	L

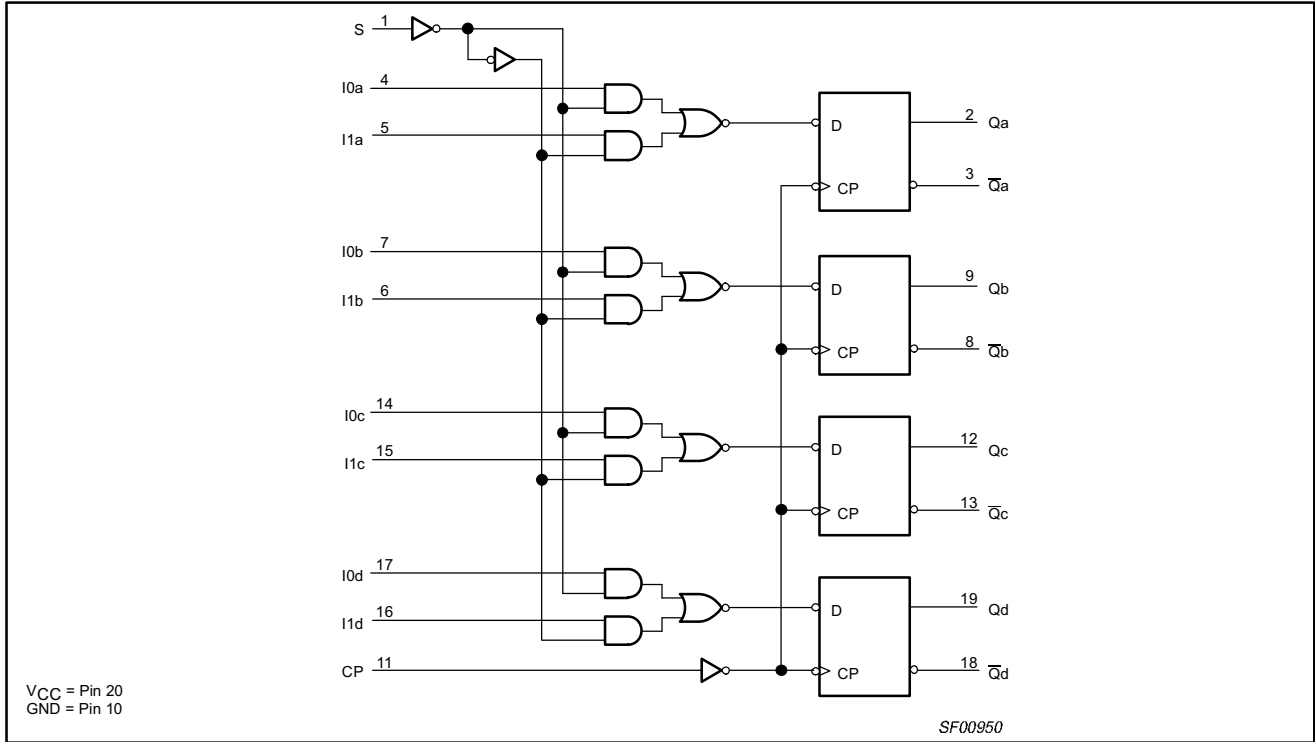
- H = High voltage level
- h = High voltage level one setup time prior to the High-to-Low clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the High-to-Low clock transition
- X = Don't care
- ↑ = Low-to-High clock transition

\* Discontinued part. Please see the Discontinued Products List.

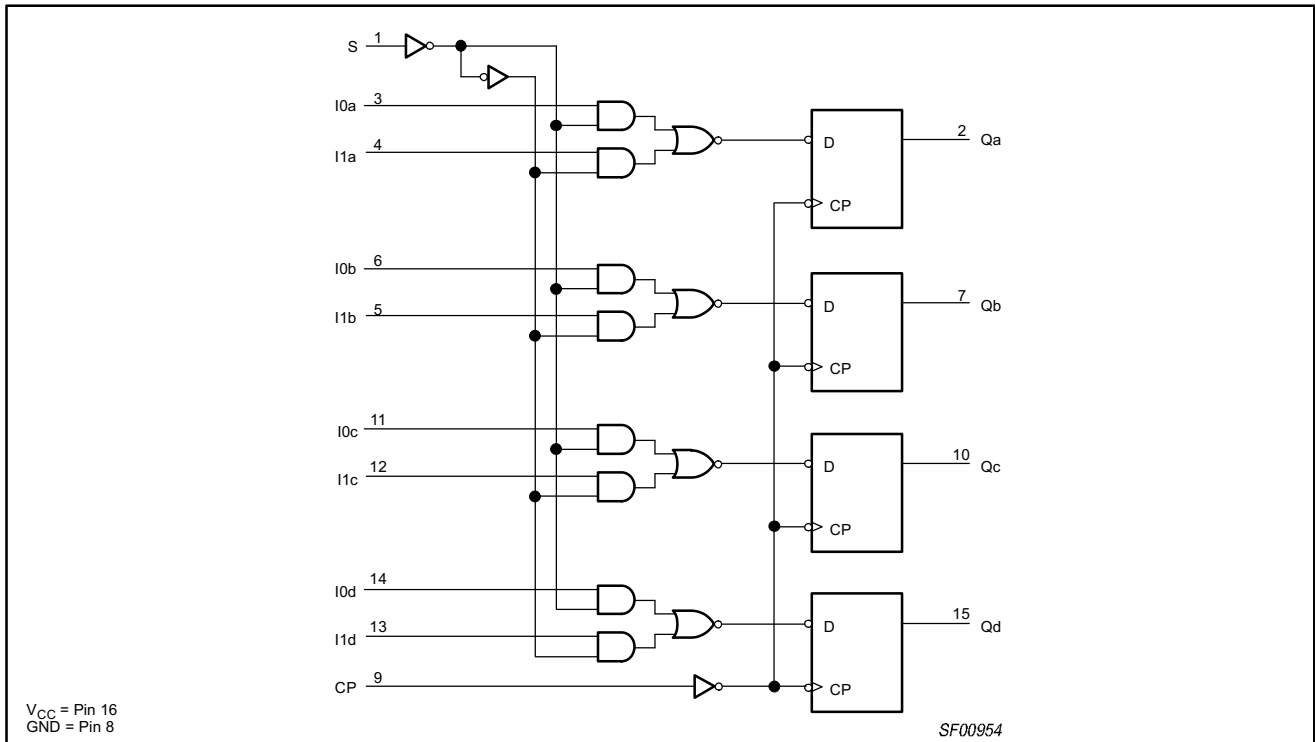
Registers

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LOGIC DIAGRAM – 74F398



LOGIC DIAGRAM – 74F399



\* Discontinued part. Please see the Discontinued Products List.

## Registers

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>	LIMITS			UNIT	
			MIN	TYP NO TAG	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
			±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
			±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>	V <sub>CC</sub> = MAX	-60		-150	mA	
I <sub>CC</sub>	Supply current (total)	74F398		25	38	mA	
		74F399		22	34	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

\* Discontinued part. Please see the Discontinued Products List.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	100	120		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn or Q̄n	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

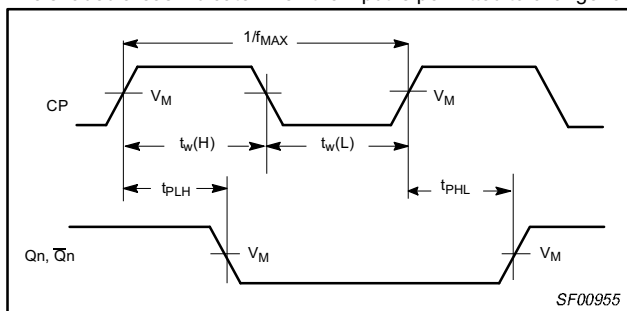
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low I0n, I1n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low I0n, I1n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

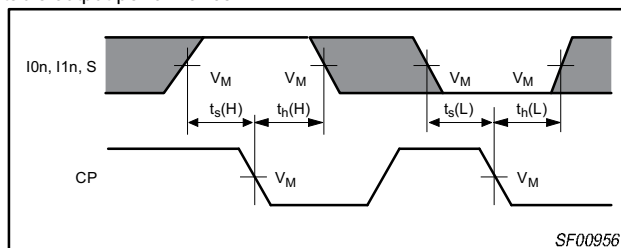
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



**Waveform 2. Data and Select Setup and Hold Times**

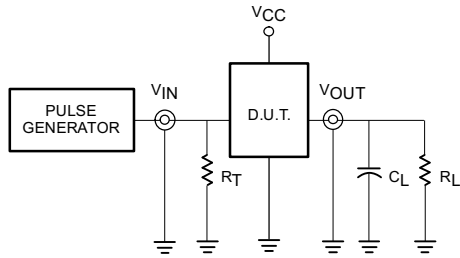
SF00956

\* Discontinued part. Please see the Discontinued Products List.

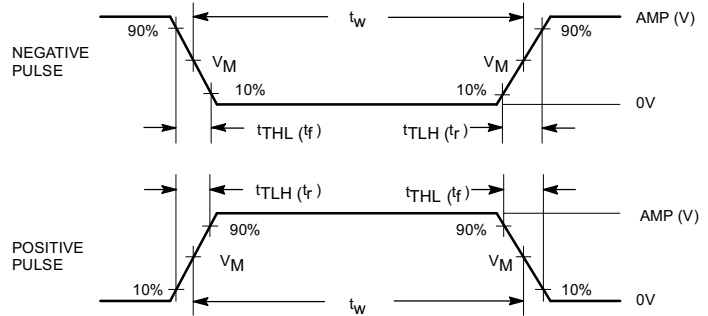
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## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}(f_r)$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

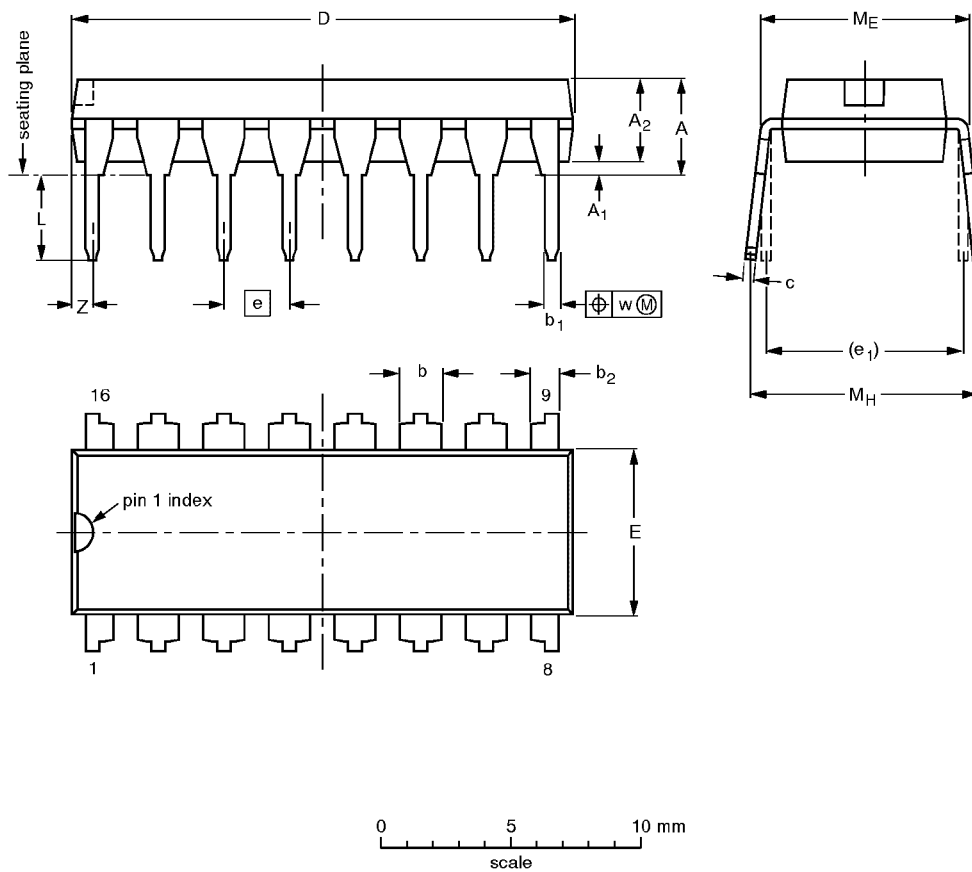
\* Discontinued part. Please see the Discontinued Products List.

Registers

74F398\*, 74F399

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

\* Discontinued part. Please see the Discontinued Product List.

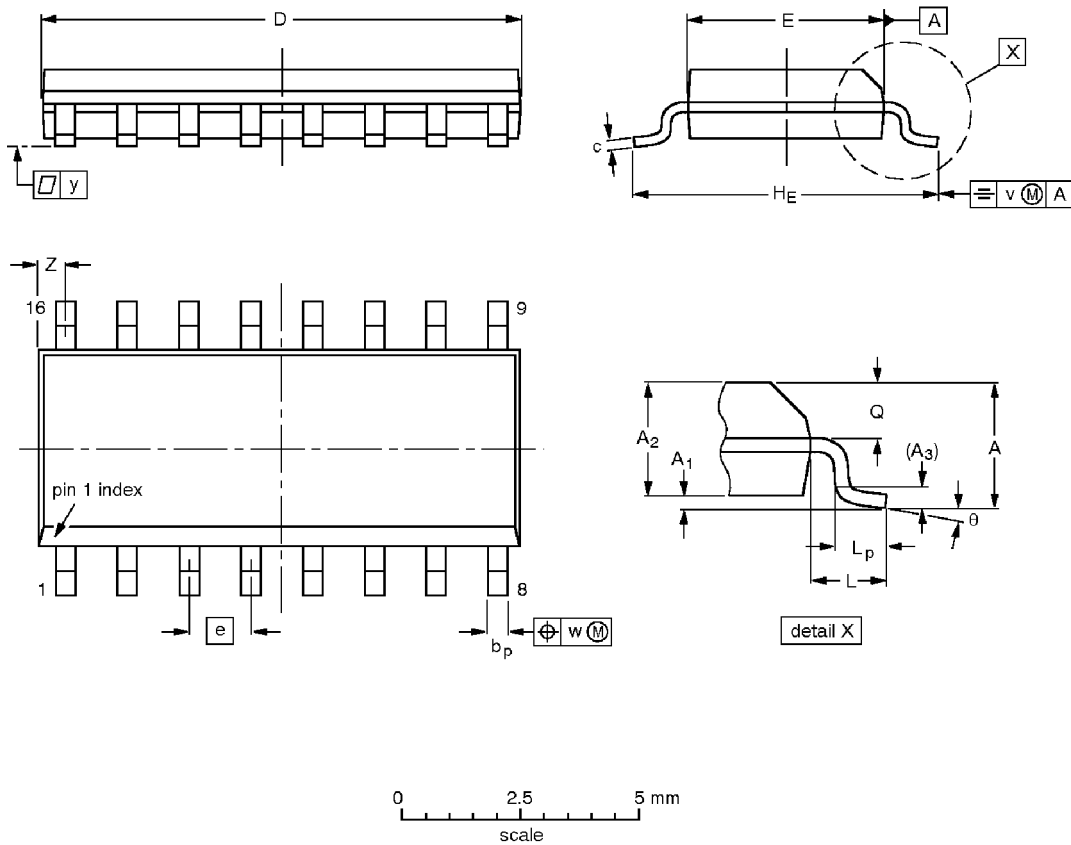


Registers

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07S	MS-012AC			95-01-23 97-05-22

\* Discontinued part. Please see the Discontinued Product List.

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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