

DATA SHEET

74F1245

Octal transceiver (3-State)

Product specification

1995 Mar 01

IC15 Data Handbook

Philips Semiconductors



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PHILIPS

Octal Transceiver (3-State)

74F1245

FEATURES

- Same function and pinout as 74F245
- High impedance NPN base inputs for reduced loading (70µA in Low and High states)
- Useful in applications where light loading bus loading or direct interface with output of a MOS microprocessor is desired
- Octal bidirectional bus interface
- Glitch free during 3-State power up and power down
- 3-State buffer outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

DESCRIPTION

The 74F1245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable (OE) input for easy cascading and Transmit/Receive (T/R) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	DRAWING NUMBER
20-Pin Plastic DIP	N74F1245N	SOT146-1
20-Pin Plastic SOL ¹	N74F1245D	SOT163-1

NOTE:

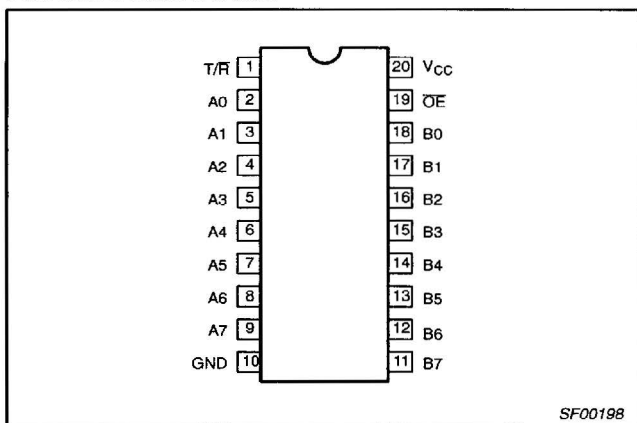
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

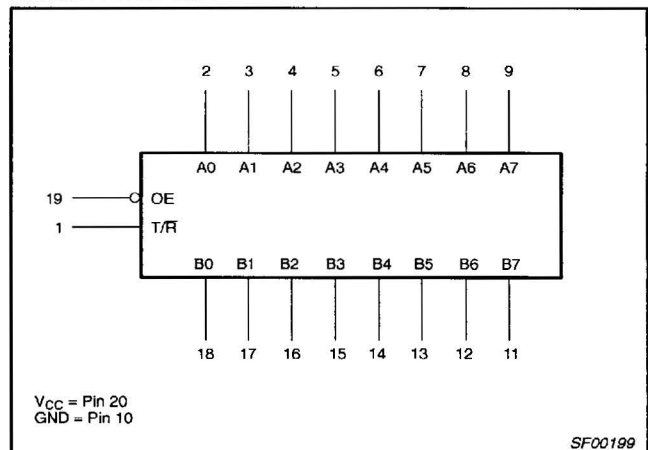
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	A and B port inputs	3.5/0.117	70µA/70µA
OE	Output Enable input (active Low)	2.0/0.033	40µA/20µA
T/R	Transmit/Receive input	2.0/0.033	40µA/20µA
A0–A7	A port outputs	150/40	3.0mA/24mA
B0–B7	B port outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



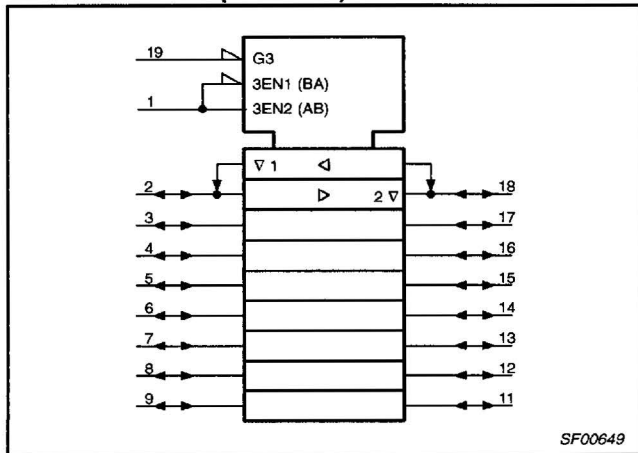
LOGIC SYMBOL



Octal Transceiver (3-State)

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LOGIC SYMBOL (IEEE/IEC)

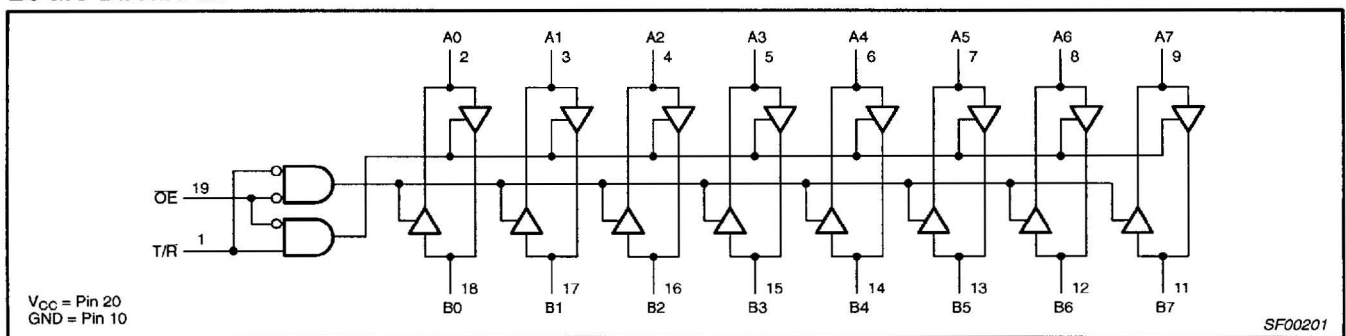


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE	T/R	An	Bn
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	Z	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

LOGIC DIAGRAM



V_{CC} = Pin 20
 GND = Pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I _{OUT}	Current applied to output in Low output state	A0-A7	48
		B0-B7	128
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current	A0-A7		-3	mA
		B0-B7		-15	mA
I _{OL}	Low-level output current	A0-A7		24	mA
		B0-B7		64	mA
T _{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT			
			MIN	TYP ²	MAX				
V _{OH}	High-level output voltage	A0-A7, B0-B7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -3mA	±10% V _{CC}	2.4		V	
					±5% V _{CC}	2.7	3.3	V	
		B0-B7	I _{OH} = -15mA	±10% V _{CC}	2.0		V		
				±5% V _{CC}	2.0		V		
V _{OL}	Low-level output voltage	A0-A7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24mA	±10% V _{CC}		0.35	0.50	V
					±5% V _{CC}		0.35	0.50	V
		B0-B7		I _{OL} = 48mA	±10% V _{CC}		0.30	0.55	V
					±5% V _{CC}		0.42	0.55	V
I _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V		
I _I	Input current at maximum input voltage	OE, T/R	V _{CC} = 0.0V, V _I = 7.0V			100	μA		
		A0-A7, B0-B7	V _{CC} = 0.0V, V _I = 5.5V			100	μA		
I _{IH}	High-level input current	OE, T/R only	V _{CC} = MAX, V _I = 2.7V			40	μA		
I _{IL}	Low-level input current	OE, T/R only	V _{CC} = MAX, V _I = 0.5V			-20	μA		
I _{IH} +I _{OZH}	Off-state output current High-level voltage applied		V _{CC} = MAX, V _O = 2.7V			70	μA		
I _{IL} +I _{OZL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V			-70	μA		
I _{OS}	Short-circuit output current ³	A0-A7	V _{CC} = MAX		-60		-150	mA	
		B0-B7			-100		-225	mA	
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			120	155	mA	
		I _{CCL}				116	150	mA	
		I _{CCZ}				110	165	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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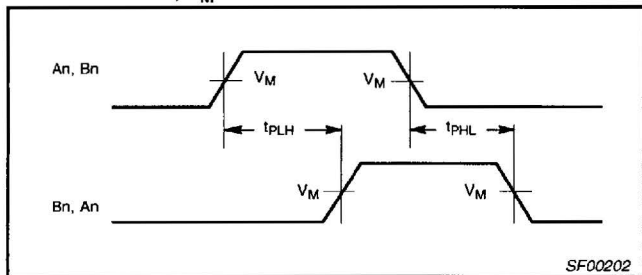
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AC ELECTRICAL CHARACTERISTICS

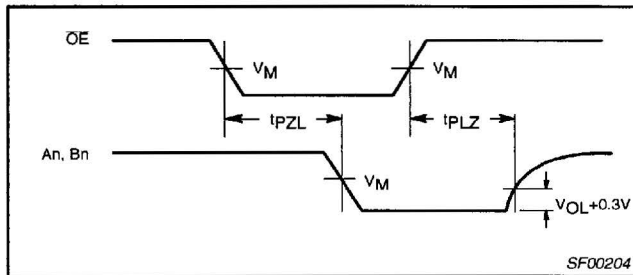
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t _{PZH} t _{PZL}	Output Enable time OE to An or Bn	Waveform 2 Waveform 3	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable time OE to An or Bn	Waveform 2 Waveform 3	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

AC WAVEFORMS

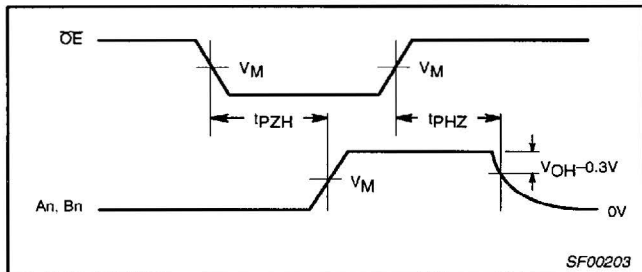
For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting Output



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

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TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition
 $V_M = 1.5V$

family	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

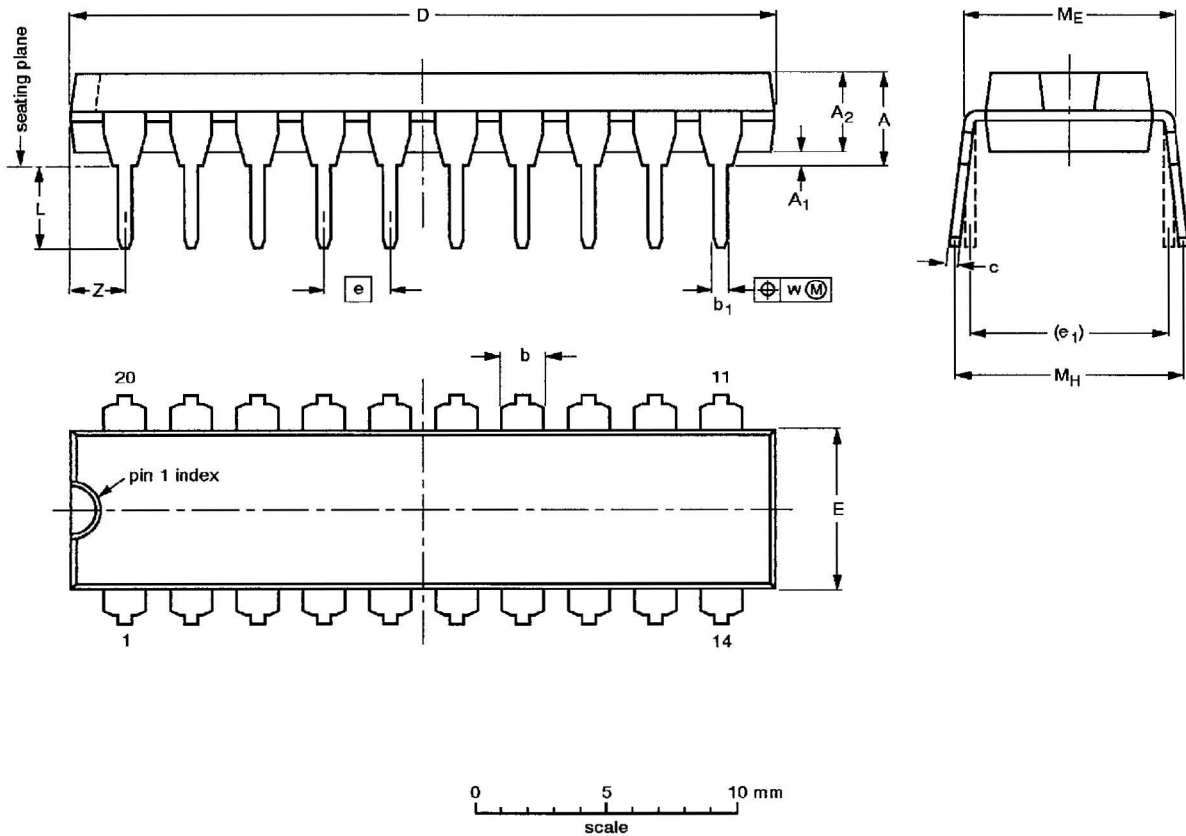
SF00333

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-01-14

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

