Octal D flip-flop 74ABT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- Power-up reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-State version
- ESD protection exceeds 2000 V per Mil Std 833 Method 3015 and 200 V per machine model.

DESCRIPTION

The 74ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	5.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} =5.5V	500	nA

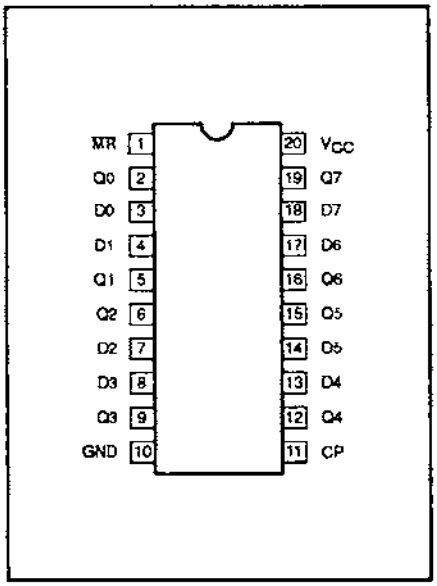
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	–40°C to +85°C	74ABT273N	0408B
20-pin plastic SOL	–40°C to +85°C	74ABT273D	0172D
20-pin plastic SSOP Type II	–40°C to +85°C	74ABT273DB	1640A

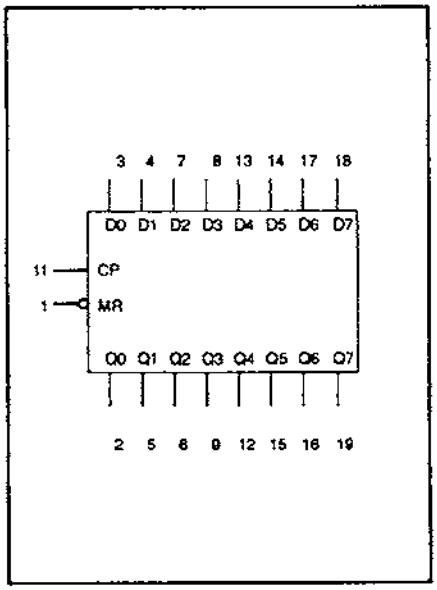
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

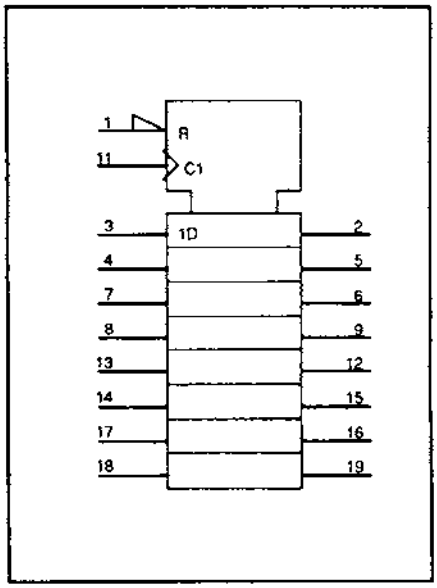
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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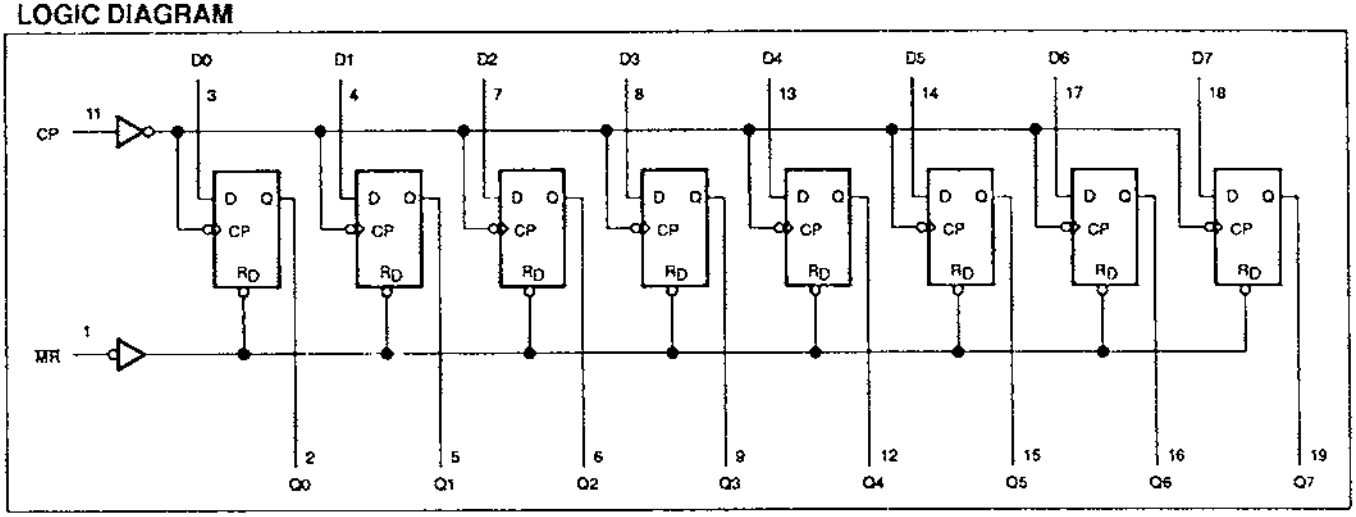
LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING
$\overline{MR}$	CP	Dn	Q0 – Q7	MODE
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low–to–High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low–to–High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low–level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	2.5 3.3	4.5 5.3	6.0 6.8	2.5 3.3	6.5 7.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	2.5	4.5	6.0	2.5	7.0	ns

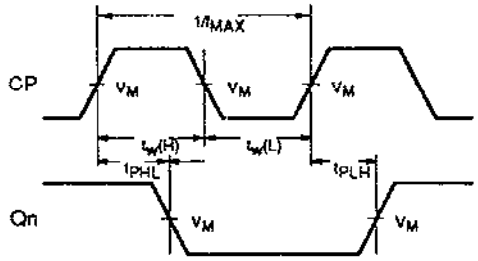
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

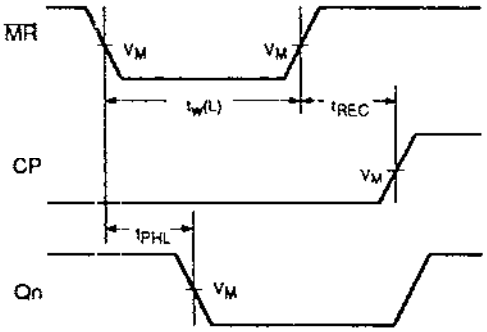
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = −40°C to +85°C V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	2.0 2.5	0.8 0.7	2.0 2.5	
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.7 0.7	−0.5 −0.5	0.7 0.7	ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	3.3 3.3	2.4 2.9	3.3 3.3	ns
$t_w(L)$	Master Reset pulse width, Low	2	3.3	2.8	3.3	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	2.0	0.7	2.0	ns

AC WAVEFORMS

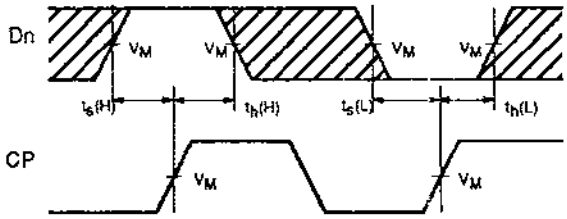
V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



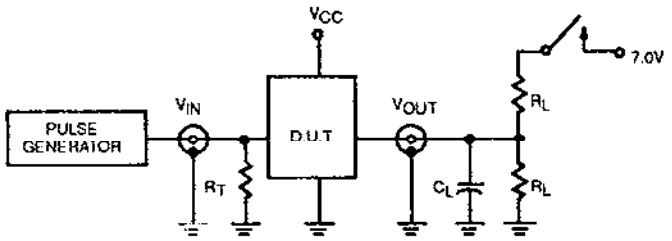
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



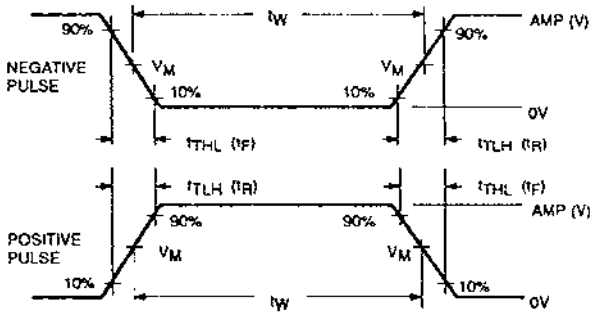
Waveform 3. Data Setup and Hold Times

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
All	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns