54/7496 016745

5-BIT SHIFT REGISTER

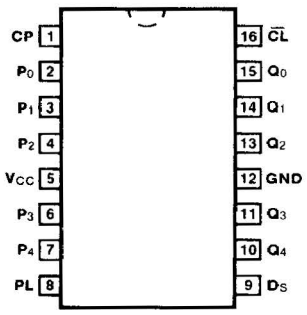
DESCRIPTION — The '96 consists of five RS master/slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the LOW state by applying a low level voltage to the clear input. This condition may be applied independent of the state of the clock input.

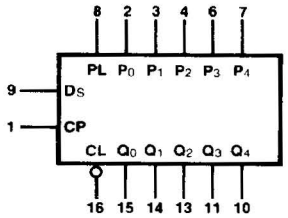
The flip-flops may be independently set to the HIGH state by applying a high level voltage to both the preset input of the specific flip-flop and the common parallel load input. The parallel enable input is provided to allow setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a LOW level to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input must be at a HIGH level and the parallel load input must be at a LOW level for serial shifting.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 5
GND= Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7496PC		9B
Ceramic DIP (D)	A	7496DC	5496DM	7B
Flatpak (F)	A	7496FC	5496FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

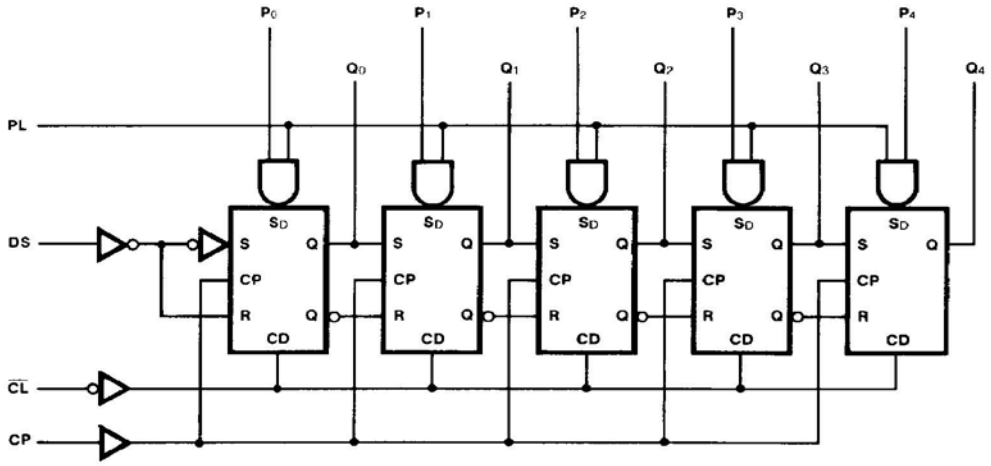
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{CL}$	Asynchronous Clear Input (Active LOW)	1.0/1.0
DS	Serial Data Input	1.0/1.0
P0 — P4	Parallel Data Inputs	1.0/1.0
PL	Asynchronous Parallel Load Input (Active HIGH)	5.0/5.0
Q0 — Q4	Parallel Outputs	10/10

MODE SELECT TABLE

INPUTS						OPERATION*
PL	P_n	$\overline{CL}$	D_S	CP	Q_n	
L	X	L	X	X	L	Clear; all outputs forced LOW
H	H**	H	X	X	H	Selectively Preset; each output
H	L**	H	X	X	L	set to its P input
L	X	H	H, L	↑	Q_{n-1}	Shift right; $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.

*Simultaneous Preset and Clear operations produce undefined states.
**To insure proper presetting, P inputs must remain stable while PL is LOW.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		68	mA	V_{CC} = Max
		XC		79		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		40 40	ns	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay, PL or P_n to Q_n		35	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay, $\overline{CL}$ to Q_n		55	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/54 Min	54/54 Max	UNITS	CONDITIONS
t_w (L)	CP Pulse Width LOW	35		ns	Fig. 3-8
t_w (L)	$\overline{CL}$ Pulse Width LOW	30		ns	Fig. 3-16
t_w (H)	PL Pulse Width HIGH	30		ns	Fig. 3-16
t_s (H)	Setup Time HIGH, D_S to CP	30		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_S to CP	0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D_S to CP	30		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_S to CP	0		ns	Fig. 3-6