1-Megabit Dynamic RAM Controller/Driver

673104
673104A

Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 16 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ delay of 23 nsec max ($\overline{\text{RAS}}$ driving 32 DRAMs)
- Max and Min skews are specified to simplify system design
- Four $\overline{\text{CASIN}}$ inputs and four $\overline{\text{CAS}}$ outputs simplify byte addressing
- An Auto-Access mode with extended $\overline{\text{CAS}}$ capability takes advantage of full performance of 120- and 150-nsec DRAMs
- An output series resistor reduces undershoot

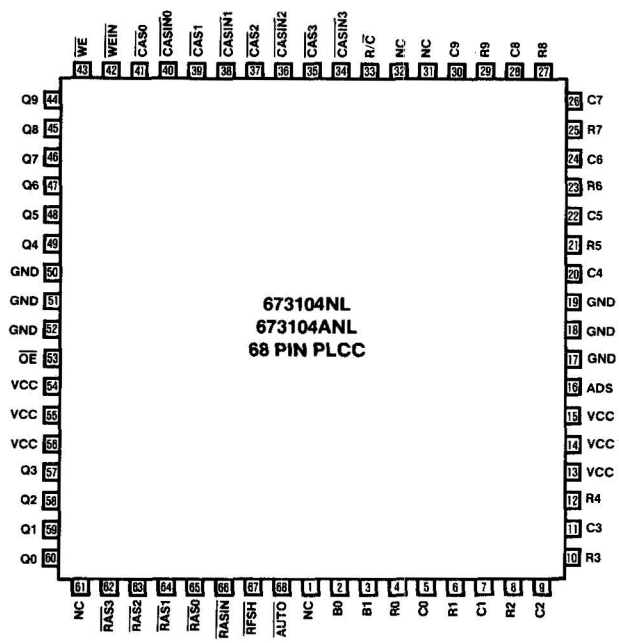
Modes of Operation

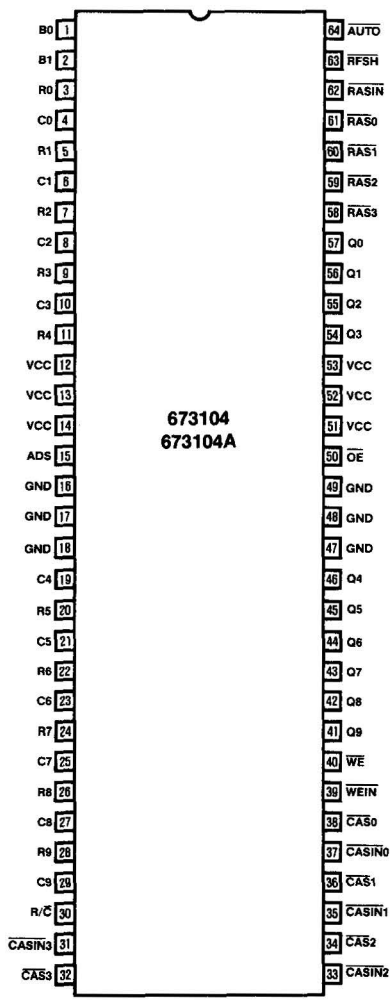
- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673104	64D, 68NL, 68NP	Com
673104A		

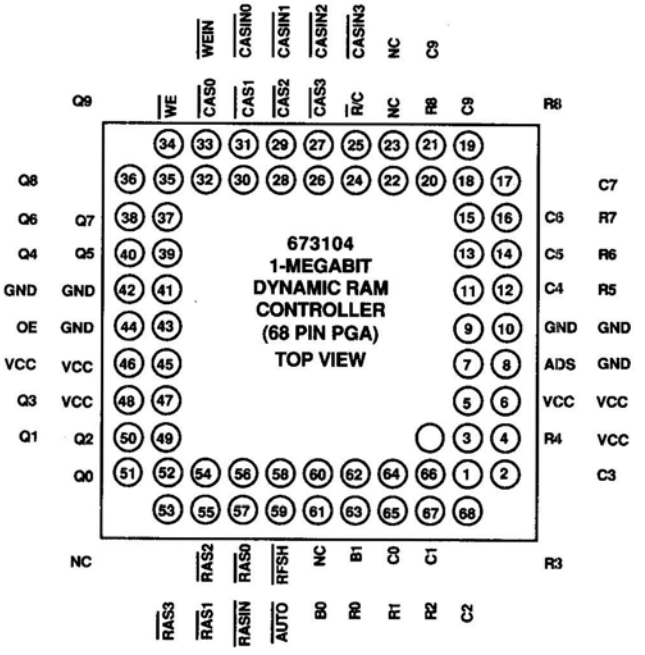
Pin Configurations





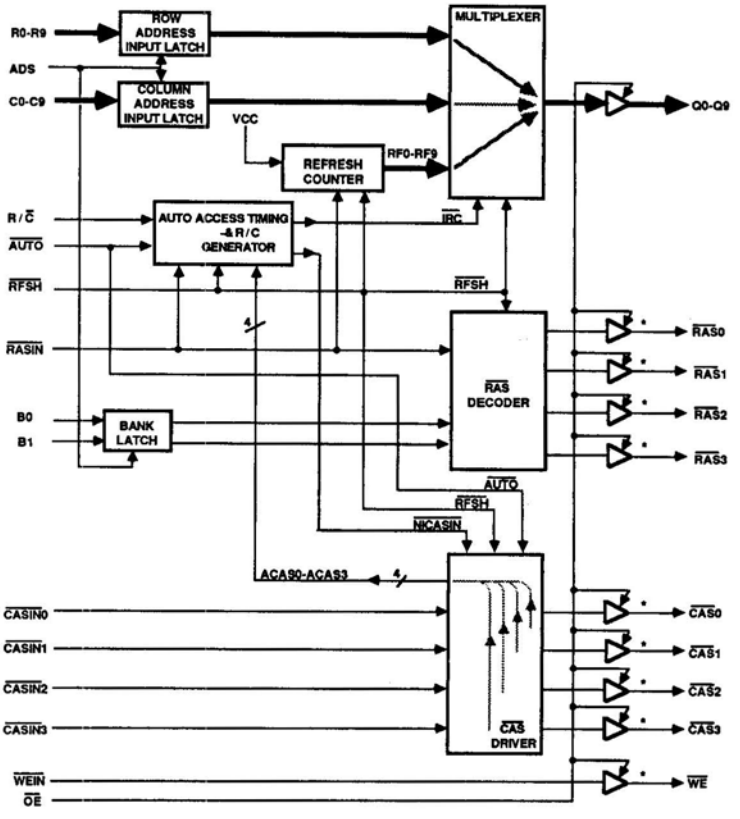
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI


WEIN
CASIN0
CASIN1
CASIN2
CASIN3
NC
C9
Q9
WE
CAS0
CAS1
CAS2
CAS3
R/C
NC
R8
C9
R8
34 33 31 29 27 25 23 21 19
Q8
36 35 32 30 28 26 24 22 20 18 17
C7
Q6
Q7
38 37
15 16
C6
R7
Q4
Q5
40 39
13 14
C5
R6
GND
GND
42 41
11 12
C4
R5
OE
GND
44 43
9 10
GND
GND
VCC
VCC
46 45
7 8
ADS
GND
Q3
VCC
48 47
5 6
VCC
VCC
Q1
Q2
50 49
3 4
R4
VCC
Q0
51 52 54 56 58 60 62 64 66 1 2
C3
53 55 57 59 61 63 65 67 68
673104
1-MEGABIT
DYNAMIC RAM
CONTROLLER
(68 PIN PGA)
TOP VIEW
NC
RAS2
RAS0
RFSH
NC
B1
C0
C1
R3
RAS3
RAS1
RASIN
AUTO
B0
R0
R1
R2
C2

9

Block Diagram



* Indicates that there is a 3-KΩ pull-up resistor on these outputs when they are disabled

Figure 1. 673104 Functional Block Diagram

Description

The 673104 is an LSI device, provided in 64-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four $\overline{RAS}$ outputs, and four $\overline{CASIN}$-$\overline{CAS}$ input-output pairs allow the 673104 to directly address 16 M bytes. The four $\overline{CASIN}$n inputs and the four $\overline{CAS}$n outputs simplify individual byte access in 32-bit wide memory arrays (see Figure 2).

The 673104 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{RAS}$m outputs, the $\overline{CAS}$n outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{RAS}$m signals, address multiplexing, and $\overline{CAS}$n signals. In the Auto-Access mode $\overline{CASIN}$0-3 inputs serve as enables for the respective $\overline{CAS}$0-3 outputs, allowing the access of any byte of the memory array (for 32-bit wide memory arrays organized in four bytes). In this mode $\overline{CAS}$0-3 outputs go HIGH only when the respective $\overline{CASIN}$0-3 inputs go HIGH, and the address switches back to row address only when $\overline{CASIN}$0-3 go HIGH. This feature allows extension of the $\overline{CAS}$ LOW time and column address time while $\overline{RASIN}$ and $\overline{RAS}$m can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected ($\overline{RFSH}$ is LOW) an on-chip refresh counter provides the refresh address; with $\overline{AUTO}$ HIGH and R/$\overline{C}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673104 can drive sixteen banks of DRAMs. $\overline{RAS}$m control signals are used to select four banks, while leaving the other twelve banks in standby. The four $\overline{CAS}$n outputs enable the selection of one bank out of four. The address lines and the $\overline{WE}$ signal can be connected to all sixteen banks. In a 32-bit wide, byte-oriented, memory array the $\overline{RAS}$m signals select one out of four banks while the $\overline{CAS}$n signals select the bytes, as shown in Figure 2.

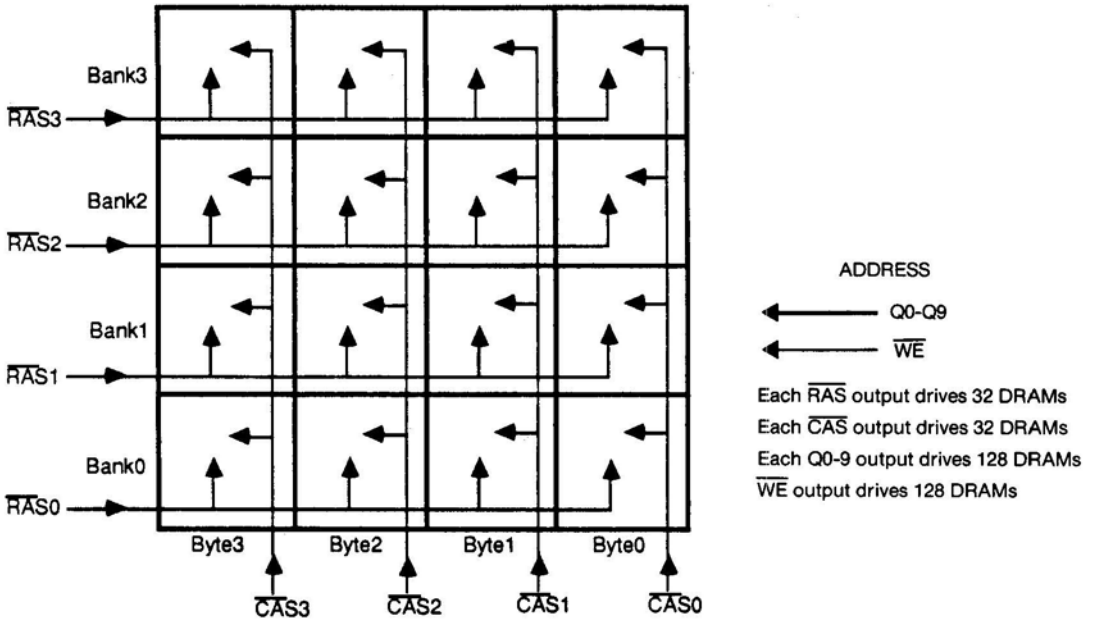


Figure 2. 673104 Addressing Four Banks of 32-bit Memory Array Organized in Four Bytes

9

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1-μF multilayer ceramic capacitor in parallel with a low voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R9: Row Address Inputs

C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes LOW in the access modes.

Q0-Q9: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

$\overline{RASIN}$: Row Address Strobe Input — Drives the selected $\overline{RAS}$m output in the access modes and all $\overline{RAS}$ outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

$\overline{OE}$: Output Enable — When $\overline{OE}$ is LOW the address and control outputs are enabled. When $\overline{OE}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/$\overline{C}$: Row/Column Select Input — In the Externally-Controlled-Access, it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{AUTO}$ is HIGH, it is used to select between the refresh address (R/$\overline{C}$ HIGH) and the column address (R/$\overline{C}$ LOW). When $\overline{AUTO}$ is LOW R/$\overline{C}$ is disabled.

$\overline{CASIN}$0-3: Column Address Strobe Inputs — In the Externally-Controlled-Access mode the $\overline{CASIN}$n directly drives $\overline{CAS}$n output. In the Auto-Access mode, it is used to enable the corresponding $\overline{CAS}$n output (See $\overline{CAS}$0-3 description).

$\overline{WEIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output.

$\overline{CAS}$0-3: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the $\overline{CAS}$ outputs follow the $\overline{CASIN}$ inputs. In the Auto-Access mode the $\overline{CASIN}$ inputs are used to enable the $\overline{CAS}$ outputs, but the $\overline{CAS}$ outputs are asserted LOW, with proper delay from the $\overline{RAS}$ output, by the $\overline{RASIN}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{CAS}$n goes HIGH only when the corresponding $\overline{CASIN}$n goes HIGH. Extending the $\overline{CAS}$n LOW duration while $\overline{RASIN}$ and $\overline{RAS}$m go HIGH satisfies the precharge requirement of the dynamic RAMs.

$\overline{RAS}$0-3: Row Address Strobe Outputs — When $\overline{RFSH}$ is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When $\overline{RFSH}$ is LOW all $\overline{RAS}$ outputs go LOW together following $\overline{RASIN}$ going LOW.

$\overline{AUTO}$: Auto-Access Input — When $\overline{AUTO}$ is LOW the Auto-Access mode is selected (see Auto-Access mode description).

$\overline{RFSH}$: Refresh Input — When $\overline{RFSH}$ is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{AUTO}$ and $\overline{RFSH}$ are held HIGH, the 673104 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{RAS}$m output selected by the B0 and B1 inputs follows the $\overline{RASIN}$ input, and each of the $\overline{CAS}$ outputs follows its corresponding $\overline{CASIN}$ input. When R/$\overline{C}$ is HIGH the row address is enabled onto the Q0-9 outputs. When R/$\overline{C}$ is LOW the column address latch is enabled onto Q0-9 outputs.

The $\overline{RASIN}$ — $\overline{RAS}$, $\overline{CASIN}$ — $\overline{CAS}$, and R/$\overline{C}$ — Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{CAS}$ before $\overline{RAS}$, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from $\overline{RASIN}$ going LOW to R/$\overline{C}$ and the delay between R/$\overline{C}$ going LOW to $\overline{CASIN}$ going LOW (see Applications).

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}$n
B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

Table 1. Memory Bank Decode

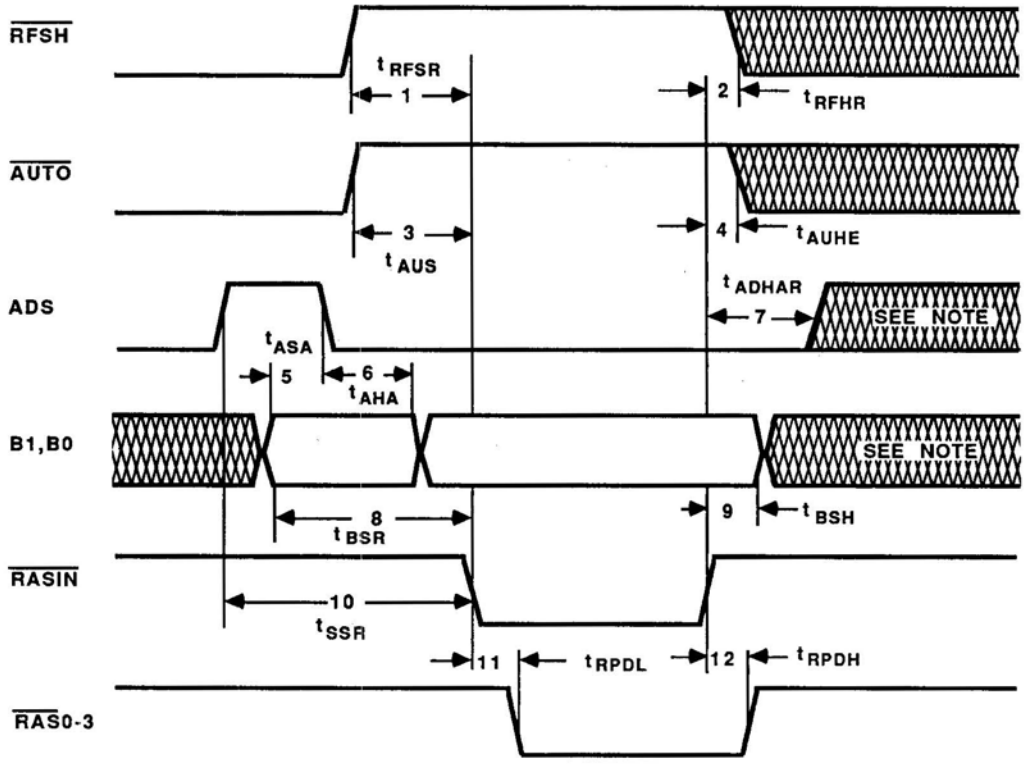


Figure 3. Externally-Controlled-Access—$\overline{RASIN}$-to-$\overline{RAS}$ Timing

Note: To prevent glitches on the $\overline{RAS}$0-3 outputs, operating conditions t_{BSH} or t_{ADHAR} must be satisfied.

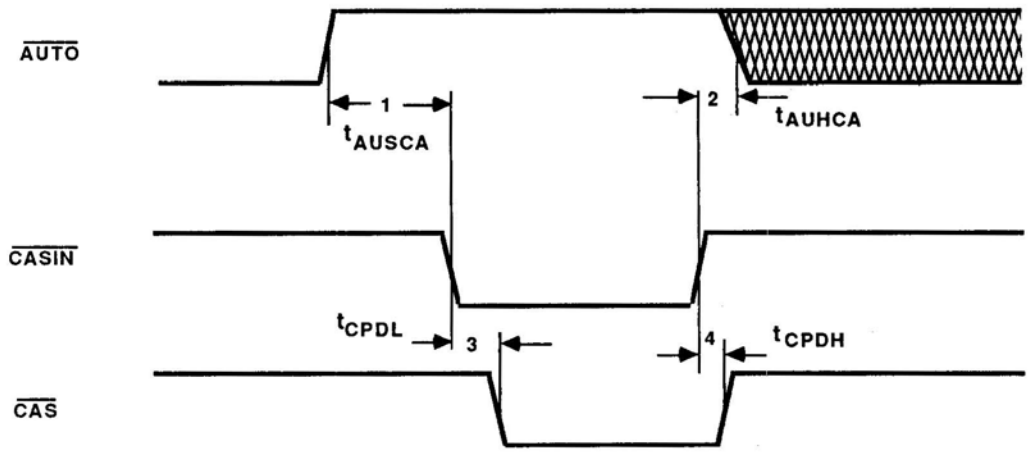


Figure 4. Externally-Controlled-Access-$\overline{\text{CASIN}}$ to $\overline{\text{CAS}}$ Timing

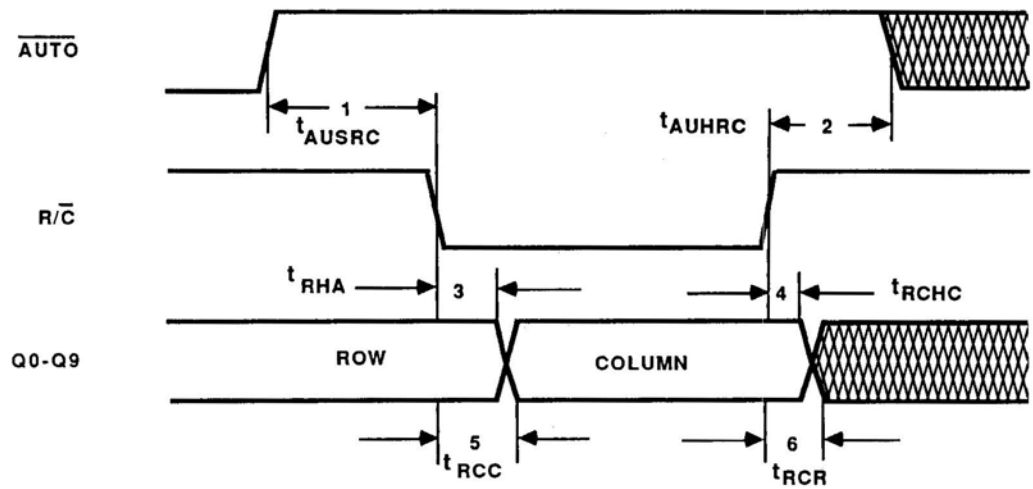


Figure 5. Externally-Controlled-Access R/$\overline{\text{C}}$ Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-9 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673104 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and RFSH is held HIGH. The R/C input is disabled, and RASIN going LOW initiates the sequence of control signals to access the DRAMs. The CASIN0-3 inputs are used as enables for the respective CAS outputs. A LOW on a CASINn input enables the CASn output to be driven LOW with the internally generated delay from RAS. Each CASn output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when all CASIN go HIGH. This feature allows extension of the CAS LOW time and the column address time, while RASIN and RASm can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.

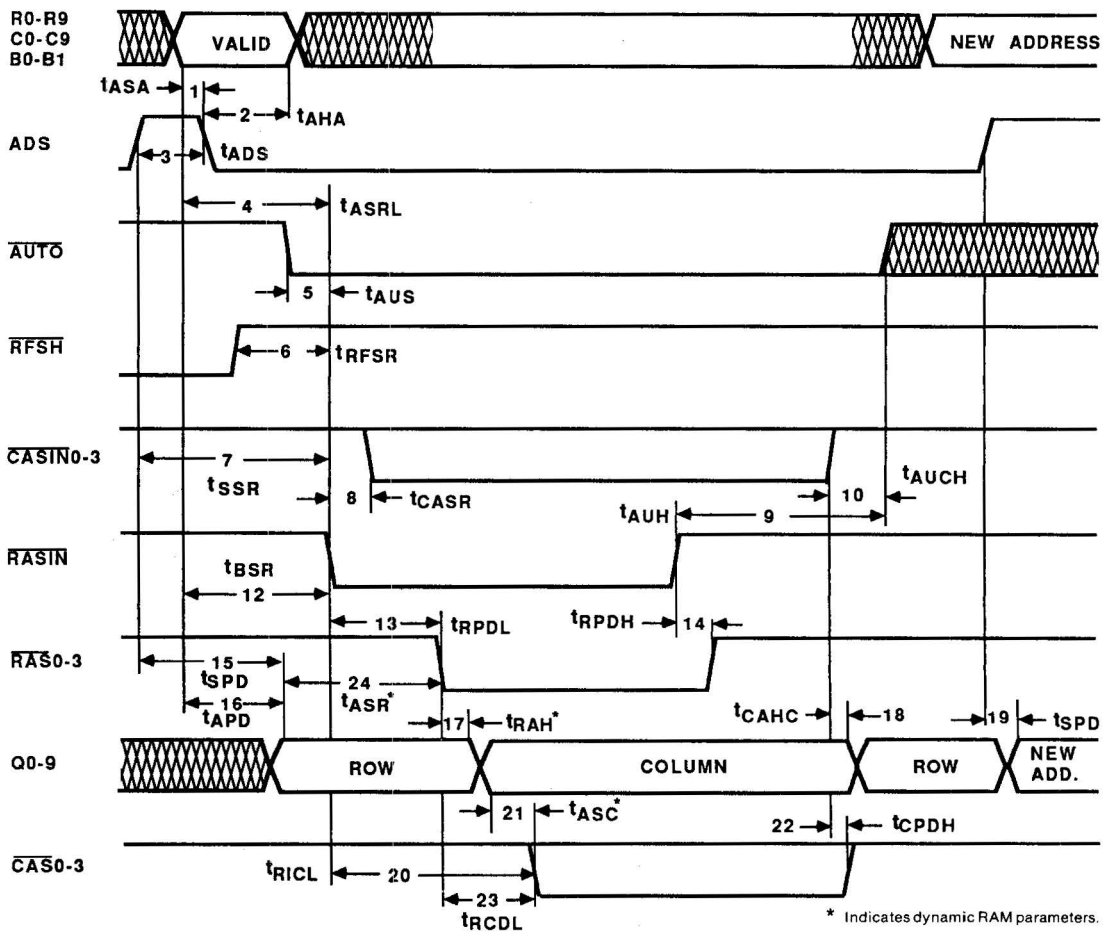


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{RFSH}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either R/$\overline{C}$ is held HIGH, or $\overline{AUTO}$ is held LOW, or both conditions exist. In this mode all four $\overline{RAS}$ outputs follow the $\overline{RASIN}$ input signal. The refresh counter increments the refresh address when either $\overline{RASIN}$ or $\overline{RFSH}$ goes HIGH while the other is LOW. When $\overline{AUTO}$ is LOW the $\overline{CASIN}$0-3 inputs are isolated and $\overline{CAS}$0-3 are held HIGH. Also, when $\overline{AUTO}$ is LOW the R/$\overline{C}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.

When $\overline{AUTO}$ is HIGH, pulling R/$\overline{C}$ LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{CAS}$ outputs follows its respective $\overline{CASIN}$ input. This feature may be used when implementing error correction and detection "scrubbing" for four-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673104 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the $\overline{CAS}$0-3 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column addresses for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on power-up and rolls-over to 0 at 1023.

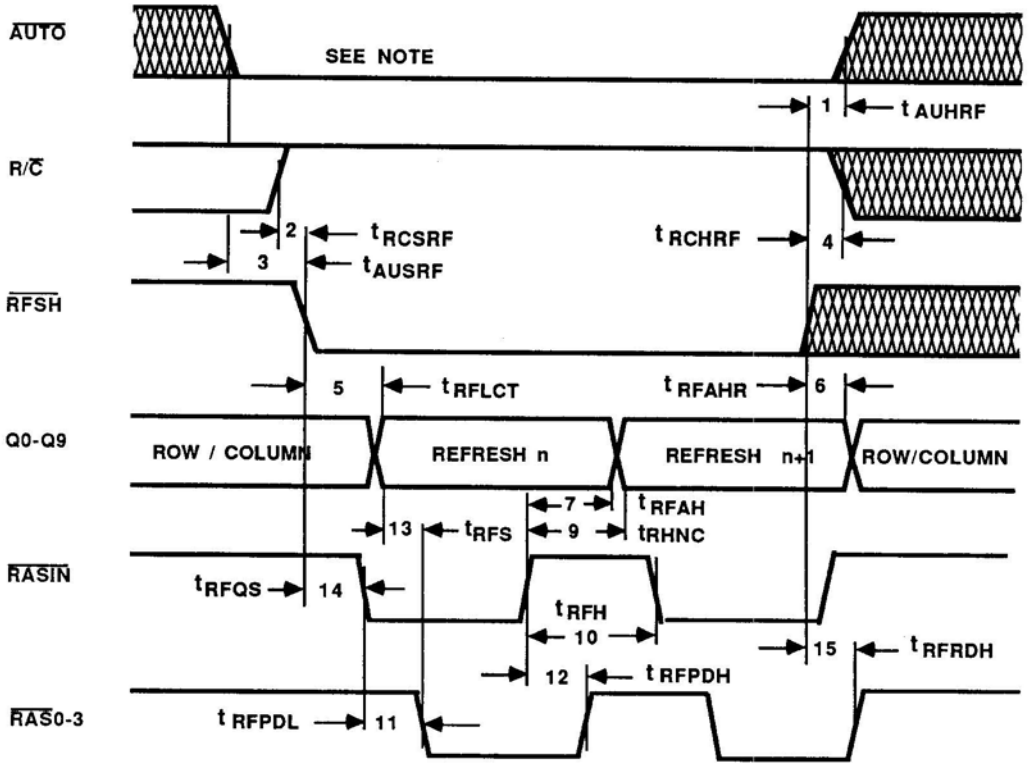


Figure 7. Refresh Timing

Note: In the REFRESH mode, $\overline{AUTO}$ must be LOW or R/$\overline{C}$ must be HIGH to guarantee the refresh address on the Q0-9 outputs.

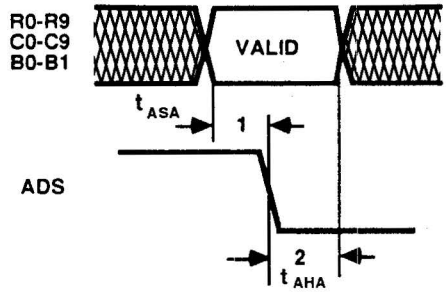


Figure 8. Address Setup and Hold Time to ADS

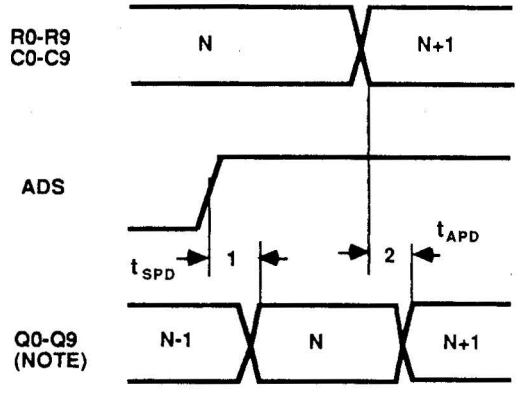


Figure 9. Address Input/Output Propagation Delay

Note: Row or Column address ($\overline{RFSH}$ = HIGH).

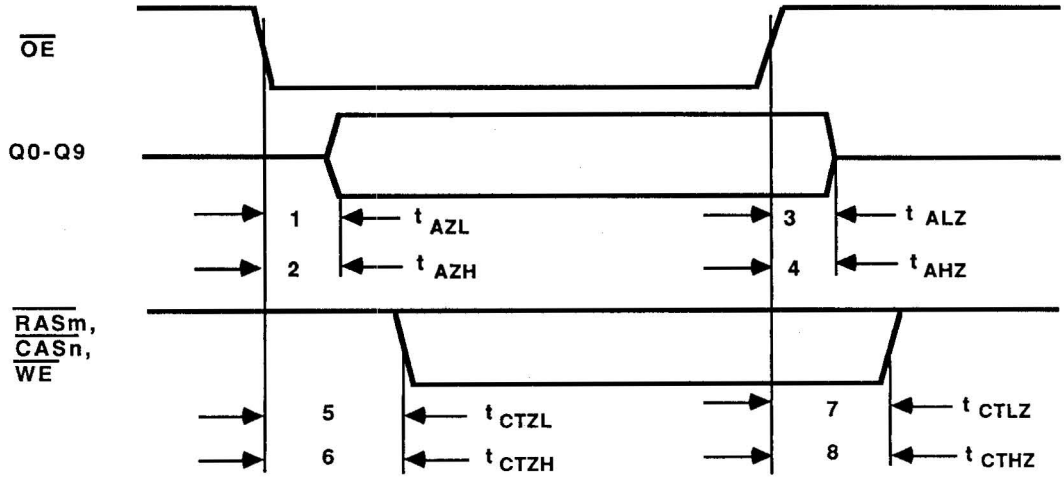


Figure 10. High-Z Timing

Absolute Maximum Ratings (See Note)

Supply voltage, V_{CC} ..... -0.5 V to 7 V
Storage temperature range ..... -65°C to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	4.5		5.5	V
T_A	Ambient temperature		0		75	0		75	C
t_{ASA}	Address setup time to ADS LOW	8/1	18			18			ns
t_{ADS}	Address strobe pulse width HIGH		26			26			ns
t_{AHA}	Address hold time from ADS LOW	8/2	10			10			ns
	EXTERNALLY CONTROLLED ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	3/8	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{SSR}	Address strobe HIGH setup to $\overline{RASIN}$ LOW (B0, B1 STABLE)	3/10	20			20			ns
t_{AUHE}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	3/4	55			55			ns
t_{AUSRC}	$\overline{AUTO}$ HIGH setup to R/$\overline{C}$ LOW	5/1	25			25			ns
t_{AUHRC}	$\overline{AUTO}$ HIGH hold from R/$\overline{C}$ HIGH	5/2	10			10			ns
t_{AUSCA}	$\overline{AUTO}$ HIGH setup to $\overline{CASIN}$ LOW	4/1	45			45			ns
t_{AUHCA}	$\overline{AUTO}$ HIGH hold from $\overline{CASIN}$ HIGH	4/2	0			0			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	3/3	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR} = 0)	3/1	10			10			ns
t_{RFHR}	$\overline{RFSH}$ HIGH hold from $\overline{RASIN}$ HIGH	3/2	10			10			ns
	AUTOMATIC ACCESS PARAMETER								
t_{ADHAR}	ADS LOW hold from $\overline{RASIN}$ HIGH	3/7	0			0			ns
t_{BSR}	Bank select setup to $\overline{RASIN}$ LOW (ADS = HIGH)	6/12	10			10			ns
t_{BSH}	Bank select hold from $\overline{RASIN}$ HIGH (ADS = HIGH)	3/9	10			10			ns
t_{ASRL}	Address setup to $\overline{RASIN}$ LOW (ADS = HIGH) (t_{ASRL} = t_{d2} max to guarantee t_{ASR} = 0)	6/4	34			34			ns
t_{AUS}	$\overline{AUTO}$ setup to $\overline{RASIN}$ LOW	6/5	0			0			ns
t_{RFSR}	$\overline{RFSH}$ HIGH setup to $\overline{RASIN}$ LOW (to guarantee t_{ASR} = 0)	6/6	10			10			ns
t_{SSR}	Address strobe HIGH to $\overline{RASIN}$ LOW (B0, B1 STABLE)	6/7	20			20			ns
t_{CASR}	$\overline{CASIN}$0-1 setup to $\overline{RASIN}$ LOW	6/8	-30			-30			ns
t_{AUH}	$\overline{AUTO}$ hold from $\overline{RASIN}$ HIGH	6/9	50			50			ns
t_{AUCH}	$\overline{AUTO}$ LOW hold from $\overline{CASIN}$ HIGH	6/10	0			0			ns
	REFRESH PARAMETER								
t_{AUHRF}	$\overline{AUTO}$ LOW hold from $\overline{RFSH}$ HIGH (R/$\overline{C}$ LOW)	7/1	10			10			ns
t_{RCSRF}	R/$\overline{C}$ HIGH setup to $\overline{RFSH}$ LOW ($\overline{AUTO}$ HIGH)	7/2	20			20			ns
t_{AUSRF}	$\overline{AUTO}$ LOW setup to $\overline{RFSH}$ LOW (R/$\overline{C}$ LOW)	7/3	20			20			ns
t_{RCHRF}	R/$\overline{C}$ HIGH hold from $\overline{RFSH}$ HIGH ($\overline{AUTO}$ HIGH)	7/4	10			10			ns
t_{RFH}	$\overline{RASIN}$ HIGH during refresh	7/10	30			30			ns
t_{RFQS}	$\overline{RFSH}$ LOW setup to $\overline{RASIN}$ LOW (to guarantee t_{RFS})	7/14	34			34			ns

9

Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤ 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN	TYP	MAX	UNIT
V_{IC}	Input clamp voltage	I_{IN} = -18 mA, V_{CC} = MIN			-0.8	-1.2	V
I_{IH}	Input high current	V_{IN} = 2.7 V, V_{CC} = MAX				50	μA
I_{CTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{OUT} = 0.4 V, V_{CC} = MAX Chip deselect			-1.5	-2.5	mA
I_{IL}	Input low current except for $\overline{RFSH}$	V_{IN} = 0.4 V, V_{CC} = MAX			-20	-250	μA
I_{ILRF}	Input low current for RFSH	V_{IN} = 0.4 V, V_{CC} = MAX			-80	-500	μA
V_{IL}	Input low threshold (Note 1)					0.8	V
V_{IH}	Input high threshold (Note 1)			2.0			V
V_{OL1}	Output low voltage	I_{OUT} = 1 mA, V_{CC} = MIN				0.5	V
V_{OL2}	Output low voltage	I_{OUT} = 12 mA, V_{CC} = MIN				0.8	V
V_{OH}	Output high voltage	I_{OUT} = -1 mA, V_{CC} = MIN		2.4	3.0		V
I_{OH}	Output source current (Note 2)	V_{OUT} = 0.8 V, V_{CC} = MIN		-50	-140		mA
I_{OL}	Output sink current (Note 2)	V_{OUT} = 2.4 V, V_{CC} = MIN		40	100		mA
I_{OZ}	Three-state output current (address output)	0.4 V ≤ V_{OUT} ≤ 2.7 V V_{CC} = MAX, Chip deselect		-50		50	μA
I_{CC}	Supply current	V_{CC} = MAX			190	280	mA
C_{IN}	Input capacitance	T_A = 25°C			10		pF

Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
t_{RHA}	Row addresses remaining valid from R/$\overline{C}$ LOW	5/3	0			0			ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	3/11			23			23	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	3/12			33			33	ns
t_{APD}	Address input to output delay	9/2			60			60	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				50			50	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				45			45	ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ LOW delay	4/3			28			28	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	4/4			40			40	ns
t_{RCC}	Column select to column address valid	5/5			50			50	ns
t_{RCR}	Row select to row address valid	5/6			53			53	ns
t_{d1}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-5		10	-5		10	ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				34			34	ns
t_{d3}	(Address input to output delay)-($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)		0		28	0		28	ns
t_{d4}	Skew between address output lines				12			12	ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-10		10	-10		10	ns
t_{d6}	($\overline{CASIN}$ to $\overline{CAS}$ LOW delay)-($\overline{CASIN}$ to $\overline{CAS}$ HIGH delay)		-12		12	-12		12	ns
t_{SPD}	ADS HIGH to address output valid	9/1			64			64	ns
t_{RCHC}	Column addresses remaining valid from R/$\overline{C}$ HIGH	5/4	0			0			ns
t_{d7}	t_{RPDL} - t_{RHA}				16			16	ns
t_{d8}	t_{RCC} - t_{CPDL}				27			27	ns

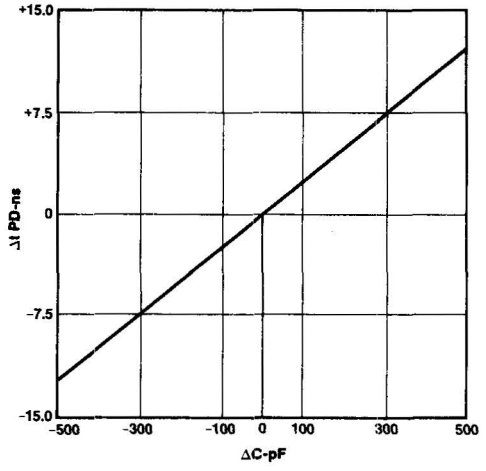
Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673104A MIN	673104A TYP	673104A MAX	673104 MIN	673104 TYP	673104 MAX	UNIT
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ LOW delay	6/20			83			90	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ LOW delay	6/23	30		73	30		80	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ LOW delay	6/13			23			23	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ HIGH delay	6/14			33			33	ns
t_{APD}	Address input to output delay	6/16			60			60	ns
t_{WPDL}	$\overline{WEIN}$ to $\overline{WE}$ LOW delay				50			50	ns
t_{WPDH}	$\overline{WEIN}$ to $\overline{WE}$ HIGH delay				45			45	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ HIGH delay	6/22			40			40	ns
t_{RAH}	Row address hold time from $\overline{RAS}$ LOW	6/17	15			15			ns
t_{d2}	(Address input to output delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)				34			34	ns
t_{SPD}	ADS HIGH to address output valid	6/19			64			64	ns
t_{ASC}	Column address setup to $\overline{CAS}$ LOW	6/21	0			0			ns
t_{CAHC}	Column address remaining valid from $\overline{CASIN}$0-3 HIGH	6/18	5			5			ns
t_{ASR}	Row address valid before $\overline{RAS}$ LOW	6/24	0			0			ns
t_{d5}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-10		10	-10		10	ns
	REFRESH PARAMETER								
t_{RFLCT}	$\overline{RFSH}$ LOW to refresh address valid ($\overline{AUTO}$ LOW or R/$\overline{C}$ HIGH)	7/5			50			50	ns
t_{RFPDL}	$\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay during refresh	7/11			26			26	ns
t_{RFPDH}	$\overline{RASIN}$ HIGH to $\overline{RAS}$ HIGH delay during refresh	7/12			38			38	ns
t_{RFAH}	Refresh address held from $\overline{RASIN}$ HIGH ($\overline{RFSH}$ LOW)	7/7	0			0			ns
t_{RHNC}	$\overline{RASIN}$ HIGH to new refresh address valid	7/9			72			72	ns
t_{RFAHR}	Refresh address held from $\overline{RFSH}$ HIGH	7/6	0			0			ns
t_{RFS}	Refresh address valid to $\overline{RAS}$ LOW (provided t_{RFQS} is satisfied)	7/13	0			0			ns
t_{RFRDH}	$\overline{RFSH}$ HIGH to $\overline{RAS}$ HIGH (for three banks, $\overline{RASIN}$ = LOW)	7/15			45			45	ns
t_{d9}	($\overline{RASIN}$ to $\overline{RAS}$ HIGH delay)-($\overline{RASIN}$ to $\overline{RAS}$ LOW delay)		-9		16	-9		16	ns
	THREE-STATE PARAMETER								
t_{AZL}	$\overline{OE}$ LOW to address output LOW	10/1			50			50	ns
t_{AZH}	$\overline{OE}$ LOW to address output HIGH	10/2			60			60	ns
t_{ALZ}	$\overline{OE}$ HIGH to address output HI-Z from LOW	10/3			35			35	ns
t_{AHZ}	$\overline{OE}$ HIGH to address output HI-Z from HIGH	10/4			25			25	ns
t_{CTZL}	$\overline{OE}$ LOW to control output LOW	10/5			50			50	ns
t_{CTZH}	$\overline{OE}$ LOW to control output HIGH	10/6			50			50	ns
t_{CTLZ}	$\overline{OE}$ HIGH to control output HI-Z from LOW	10/7			35			35	ns
t_{CTHZ}	$\overline{OE}$ HIGH to control output HI-Z from HIGH	10/8			30			30	ns

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

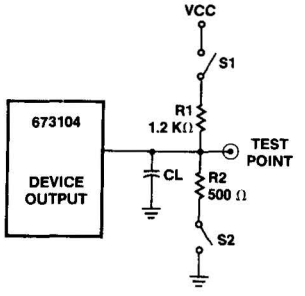
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 32 DRAMs with trace capacitance. The values are: Q0-8 C_L = 800 pF, $\overline{RAS}$0-3 C_L = 250 pF, $\overline{WE}$ C_L = 800 pF, $\overline{CAS}$0-3 C_L = 300 pF.



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load

673104 Test Loads (See Note)



Note: Input pulse 0 V to 3.0 V, $t_R = t_F$ = 2.5 ns, f = 1.0 MHz, t_{PW} = 200 ns.
Input reference point on AC measurements is 1.5 V.
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

Address Outputs

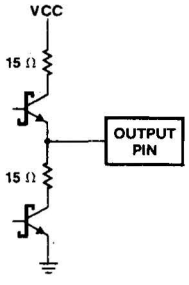
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	800 pF	0.8 V, 2.4 V
t_{PZH}	Closed	Closed	800 pF	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Closed	Closed	800 pF	0.8 V
t_{PLZ}	Closed	Open	15 pF	V_{OL} +0.5 V

Control Outputs

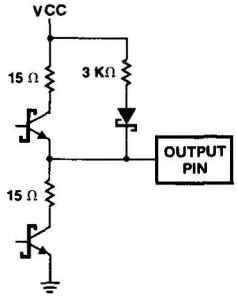
TEST	S1	S2	CL	MEASURED AT
t_{PD}	Open	Closed	CL	0.8 V, 2.4 V
t_{PZH}	Open	Closed	CL	2.4 V
t_{PHZ}	Open	Closed	15 pF	V_{OH} -0.5 V
t_{PZL}	Open	Open	CL	0.8 V
t_{PLZ}	Open	Open	15 pF	V_{OL} +0.5 V

Where C_L = 250 pF for $\overline{RAS}$, 300 pF for $\overline{CAS}$, and 800 pF for $\overline{WE}$.

Address Driver Output Stage



Control Driver Output Stage



Applications

Microprocessor Interface

The 673104 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 32-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. For some microprocessors external logic is required also to decode the address and control signal to arrive at four data strobes. A hidden refresh (refresh which is transparent to the system) scheme may be implemented in the interface circuitry taking advantage of "free" system time to refresh the memory, and falling back to "forced" refresh when hidden refresh cannot be performed.

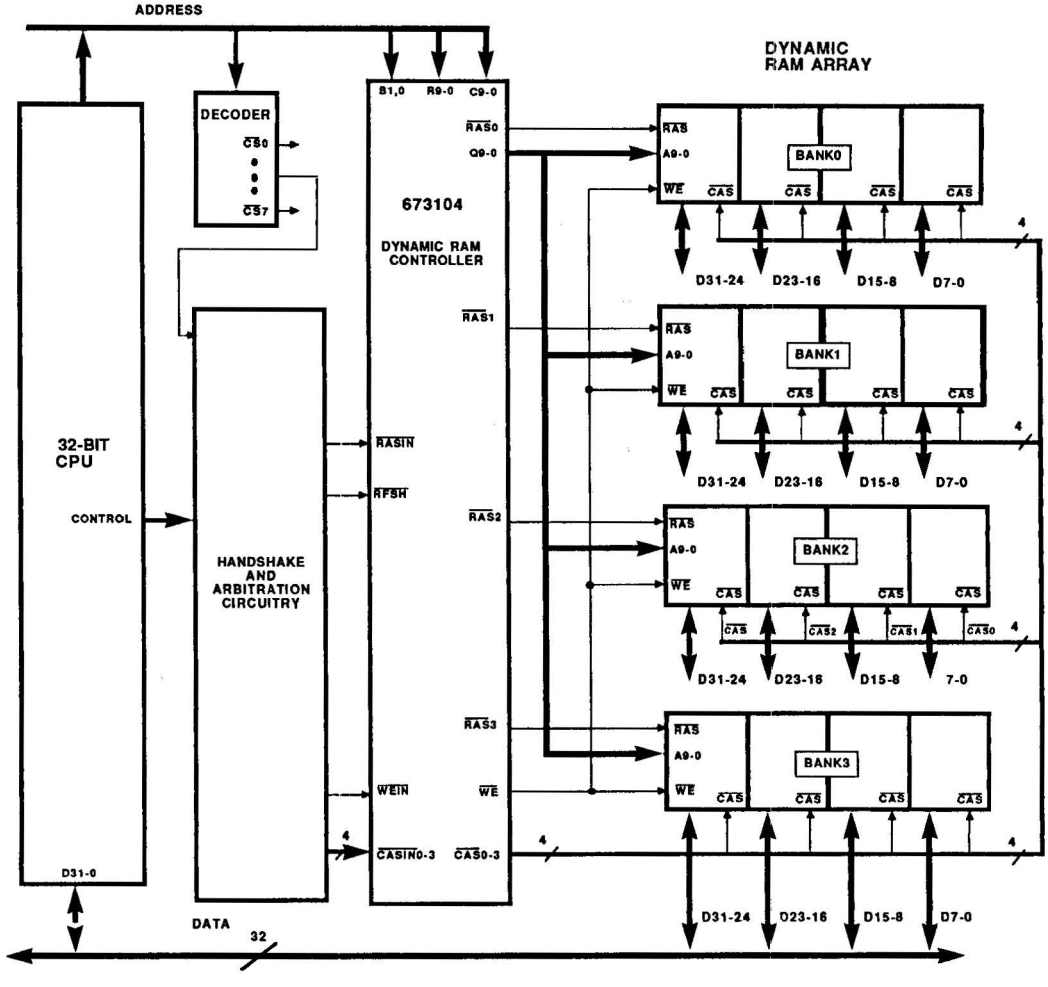


Figure 1. A CPU Interfaced to the 673104 Driving 16 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} ($\overline{RAS}$ access time) from $\overline{RAS}$ going LOW or t_{CAC} ($\overline{CAS}$ access time) from $\overline{CAS}$ going LOW. Since the $\overline{RAS}$ and $\overline{CAS}$ coming out of the controller are initiated by the $\overline{RASIN}$, the controller-memory performance is measured from the $\overline{RASIN}$ HIGH-to-LOW transition (see Figure 2).

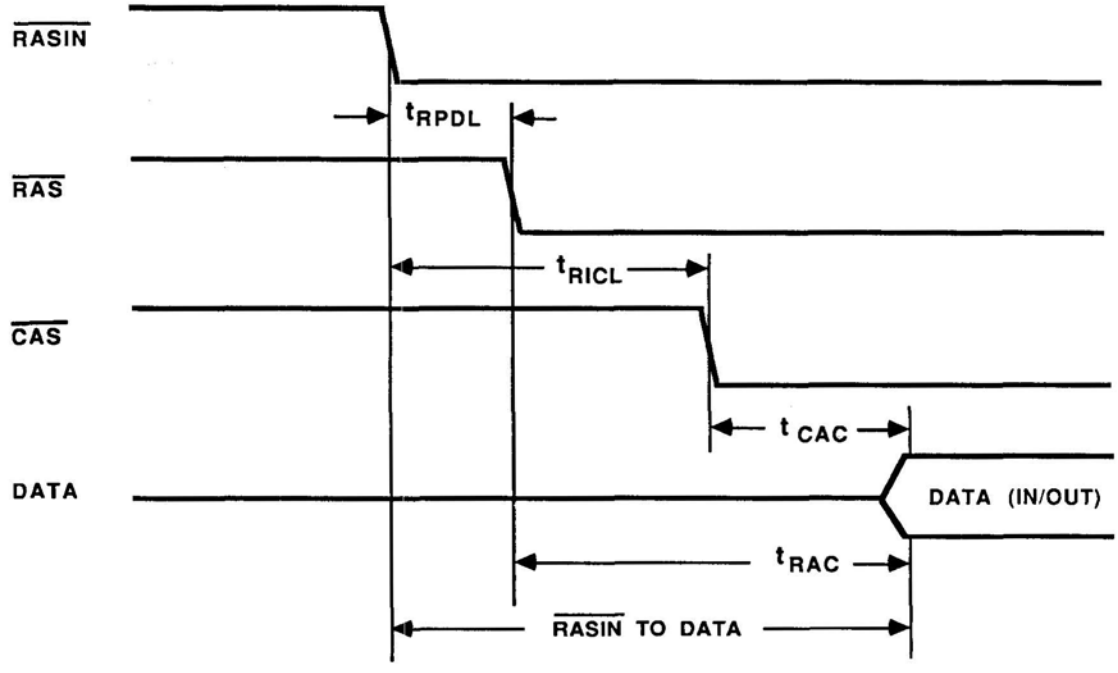


Figure 2. Access Time from $\overline{RASIN}$

The time from $\overline{RASIN}$ to data is calculated to be the longer of:

$t_{RICL} + t_{CAC}$ ($\overline{RASIN}$ to $\overline{CAS}$ + $\overline{CAS}$ to data)

$t_{RPDL} + t_{RAC}$ ($\overline{RASIN}$ to $\overline{RAS}$ + $\overline{RAS}$ to data)

Table 1 illustrates the access times from $\overline{RASIN}$ achieved for various dynamic RAM speeds.

CONTROLLER/MEMORY	PARAMETER				
	t_{RAC}	t_{RPDL}	t_{CAC}	t_{RICL}	ACCESS TIME FROM $\overline{RASIN}$
673104/HM256-12	120	23	60	90	150
673104A/HM256-12	120	23	60	83	143
673104/HM256-15	150	23	75	90	173
673104A/HM256-15	150	23	75	83	173
673104/MB8265A-10	100	23	50	90	140
673104A/MB8265A-10	100	23	50	83	133
673104/MB8265A-12	120	23	60	90	150
673104A/MB8265A-12	120	23	60	83	143
673104/IMS2620-10	100	23	60	90	150
673104A/IMS2620-10	100	23	60	83	143
673104/IMS2620-12	120	23	70	90	160
673104A/IMS2620-12	120	23	70	83	153

Table 1. Access Times from $\overline{RASIN}$ for Various Memory Speeds

673104 Parameters

t_{RICL} — $\overline{RASIN}$ LOW to $\overline{CAS}$ LOW delay

t_{RPDL} — $\overline{RASIN}$ LOW to $\overline{RAS}$ LOW delay

DRAM Parameters

t_{RAC} — Access time from $\overline{RAS}$ LOW

t_{CAC} — Access time from $\overline{CAS}$ LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode $\overline{RASIN}$ controls the selected $\overline{RAS}$ output, $\overline{CASIN}$0-3 control $\overline{CAS}$0-3 outputs respectively and R/$\overline{C}$ controls the address multiplexer. The system designer may create, using the $\overline{RASIN}$, $\overline{CASIN}$ and R/$\overline{C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

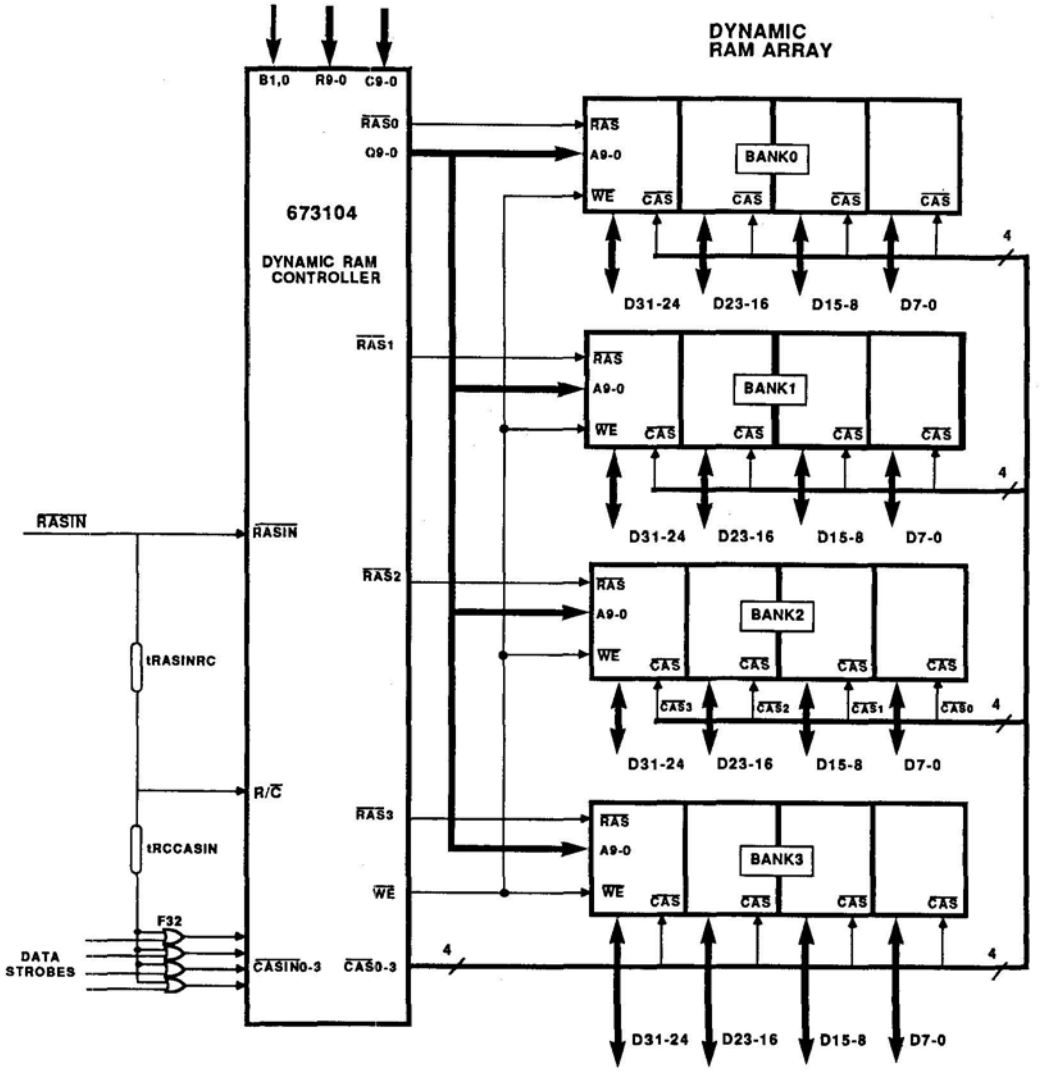


Figure 3. The 673104 in the Externally-Controlled Access Mode

Externally Controlled Access (ECA)
(Continued)

Example 1: Computing $\overline{RASIN}$ to R/$\overline{C}$ Delay

The delay between $\overline{RASIN}$ going LOW to R/C going LOW ($t_{RASINRC}$) which is required in order to satisfy the dynamic RAMs' row address hold time (t_{RAH}) is computed as follows:

$t_{RASINRC} = t_{RAH}(min) + t_{d7}$

Where:

$t_{RAH}(min)$ — Row address hold time (dynamic RAM parameter)

$t_{d7}(max) = t_{RPDL} - t_{RHA}$

t_{RPDL} — $\overline{RASIN}$ to $\overline{RAS}$ LOW delay

t_{RHA} — Row address held valid from R/$\overline{C}$ LOW

Example 2: Computing R/$\overline{C}$ to $\overline{CASIN}$ Delay

The delay between R/$\overline{C}$ going LOW and $\overline{CASIN}$ going LOW ($t_{RCCASIN}$) which is required in order to satisfy the dynamic RAMs' column address setup (t_{ASC}) is computed as follows:

$t_{RCCASIN} = t_{ASC}(min) + t_{d8} + t_{PD}F32(max)$

Where:

$t_{ASC}(min)$ — Column address setup (dynamic RAM parameter)

$t_{d8}(max) = t_{RCC} - t_{CPDL}$

t_{RCC} — R/$\overline{C}$ low to column address valid

t_{CPDL} — $\overline{CASIN}$ to $\overline{CAS}$ LOW delay

$t_{PD}F32(max)$ — Propagation delay of the OR gate used to validate $\overline{CASIN}$

Better system performance may be achieved using the t_{d7}, t_{d8} switching parameters to calculate $t_{RASINRC}$ and $t_{RCCASIN}$ than when using the t_{RPDL}, t_{RCDL}, t_{RCC} and t_{RHA} parameters (see Externally Controlled Access switching parameters).

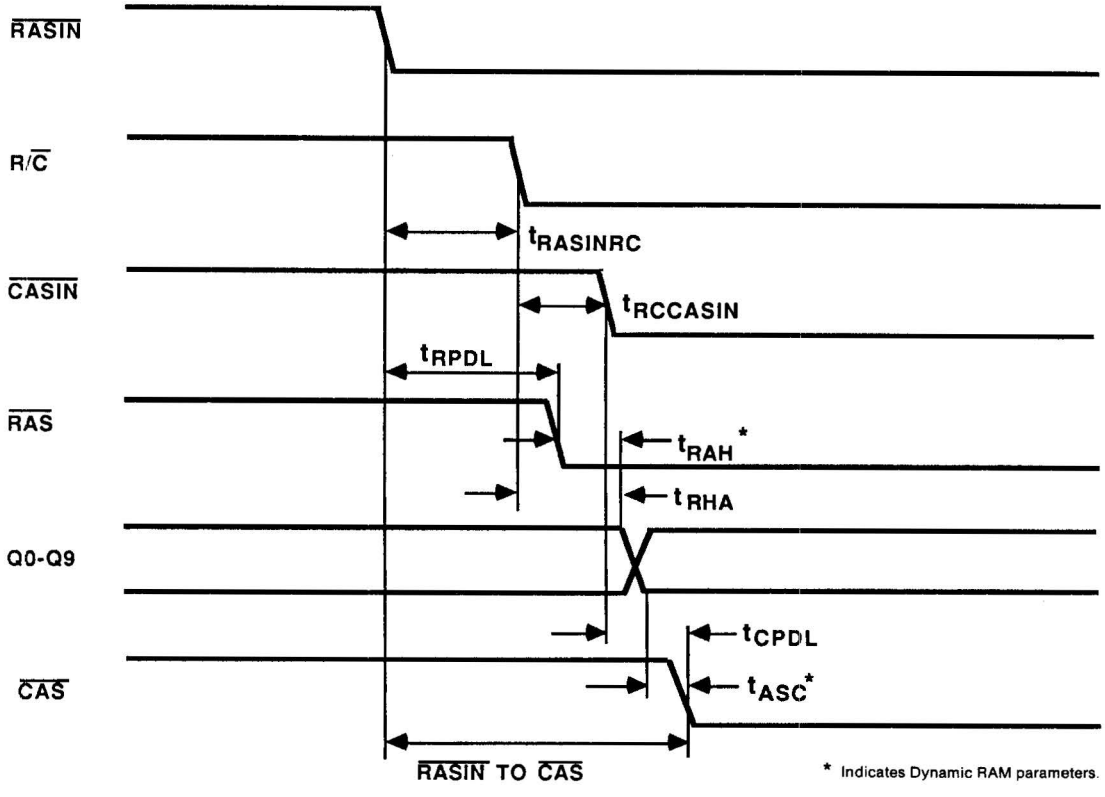


Figure 4. Externally Controlled Access Timing