4555B • 4556B

DUAL 1-OF-4 DECODERS/DEMULTIPLEXERS

DESCRIPTION — The 4555B and 4556B are Dual 1-of-4 Decoders/Demultiplexers. Each decoder/demultiplexer has two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and four mutually exclusive Outputs which are active HIGH for the 4555B (O_0-O_3) and active LOW for the 4556B ($\overline{O}_0$-$\overline{O}_3$).

When the 4555B is used as a decoder, the Enable Input ($\overline{E}$) when HIGH, forces all Outputs (O_0-O_3) LOW. When used as a demultiplexer, the appropriate Output is selected by the Data on the Address Inputs (A_0, A_1) and follows as the inverse of the Enable Input ($\overline{E}$). All unselected Outputs are LOW.

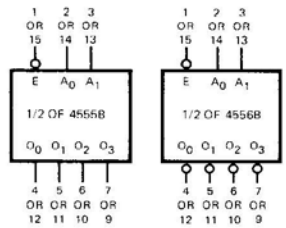
When the 4556B is used as a decoder, the Enable Input ($\overline{E}$) when HIGH forces all Outputs ($\overline{O}_0$-$\overline{O}_3$) HIGH. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows the state of the Enable Input ($\overline{E}$). All unselected Outputs are HIGH.

- **ACTIVE HIGH OUTPUTS FOR THE 4555B AND ACTIVE LOW OUTPUTS FOR THE 4556B**
- **OVERRIDING ACTIVE LOW ENABLE**

PIN NAMES

$\overline{E}$	Enable Input (Active LOW)
A_0, A_1	Address Inputs
O_0-O_3	Outputs (Active HIGH — 4555B Only)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW — 4556B Only)

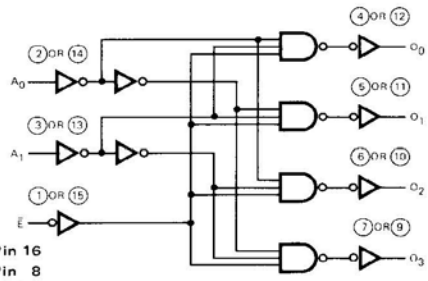
LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

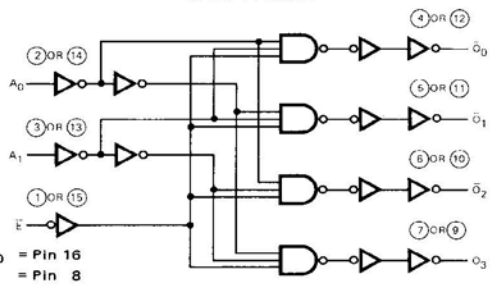
LOGIC DIAGRAMS

1/2 OF A 4555B



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

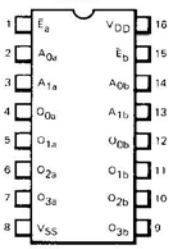
1/2 OF A 4556B



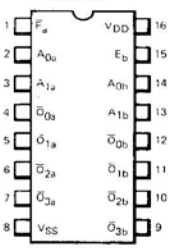
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)

4555B



4556B



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4555B TRUTH TABLE

$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

4556B TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4555B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Address to Output		148	285		60	145		40	116	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			127	265		54	120		45	96		
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		148	315		60	150		40	120	ns	
t_{PHL}			127	295		53	140		40	112		
t_{TLH}	Output Transition Time		65	135		20	70		25	45	ns	
t_{THL}			66	135		25	70		20	45		

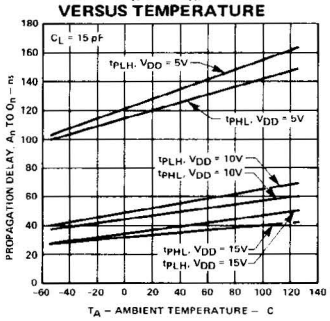
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, 4556B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Address to Output		140	225		57	100		40	80	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			185	260		68	120		45	96		
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		134	225		55	110		40	88	ns	
t_{PHL}			145	245		58	110		40	88		
t_{TLH}	Output Transition Time		75	135		37	70		25	45	ns	
t_{THL}			77	135		29	70		20	45		

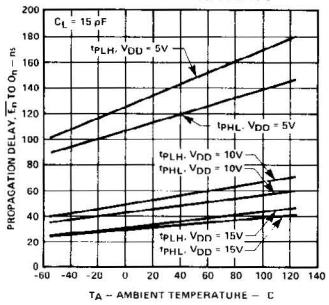
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

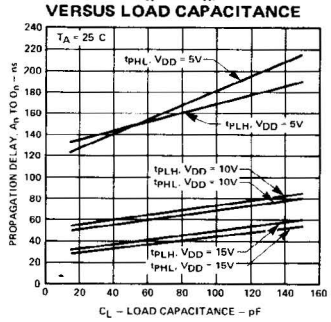
4555B PROPAGATION DELAY, A_n TO O_n, VERSUS TEMPERATURE



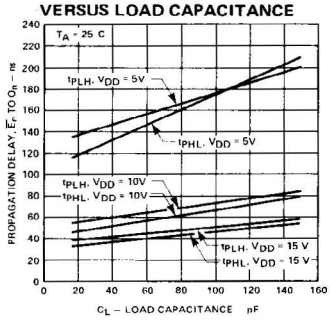
4555B PROPAGATION DELAY, $\overline{E_n}$ TO O_n, VERSUS TEMPERATURE



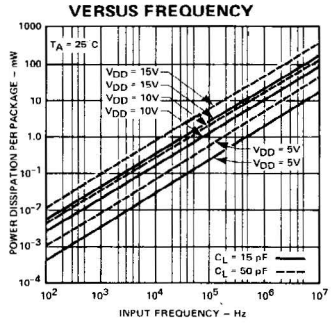
PROPAGATION DELAY, A_n TO O_n, VERSUS LOAD CAPACITANCE



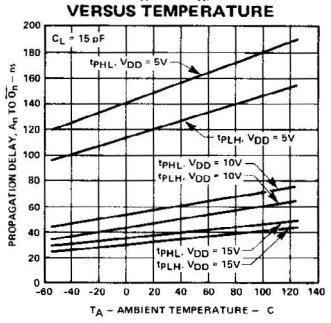
4555B PROPAGATION DELAY, $\overline{E_n}$ TO O_n, VERSUS LOAD CAPACITANCE



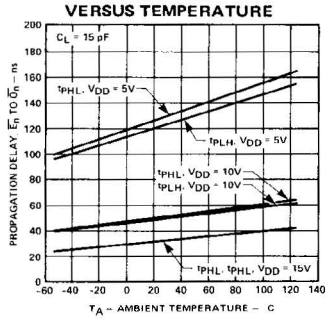
4555B AND 4556B POWER DISSIPATION VERSUS FREQUENCY



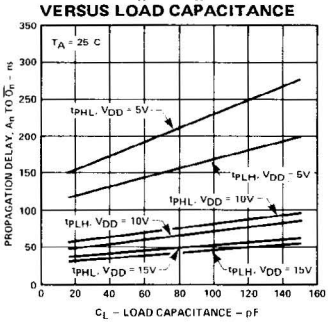
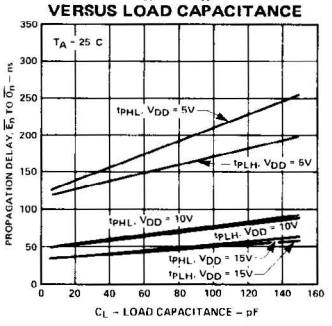
4556B PROPAGATION DELAY, A_n TO $\overline{O_n}$, VERSUS TEMPERATURE



4556B PROPAGATION DELAY, $\overline{E_n}$ TO $\overline{O_n}$, VERSUS TEMPERATURE



4556B PROPAGATION DELAY, A_n TO $\overline{O_n}$ VERSUS LOAD CAPACITANCE



4556B PROPAGATION DELAY, $\overline{E_n}$ TO $\overline{O_n}$, VERSUS LOAD CAPACITANCE