

CD4532B Types

CMOS 8-Bit Priority Encoder

High-Voltage Types (20-Volt Rating)

The RCA-CD4532B consists of combination logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_1 is low. When E_1 is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_0) is high when no priority inputs are present. If any one input is high, E_0 is low and all cascaded lower-order stages are disabled.

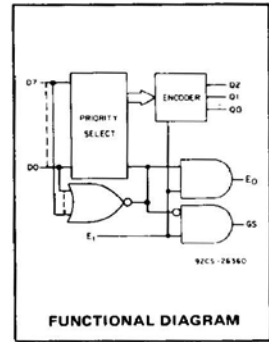
The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Converts from 1 of 8 to binary
- Provides cascading feature to handle any number of inputs
- Group select indicates one or more priority inputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1 \mu\text{A}$ at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range):
 - 1 V at $V_{DD} = 5 \text{ V}$
 - 2 V at $V_{DD} = 10 \text{ V}$
 - 2.5 V at $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic

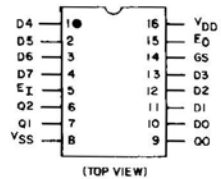


RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for $T_A = \text{Full Package Temp. Range}$)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5 \text{ V}$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10 \text{ mA}$
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING): At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79 \text{ mm}$) from case for 10 s max.	$+265^\circ\text{C}$



TERMINAL ASSIGNMENT

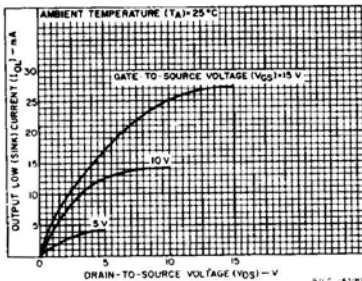


Fig. 1 — Typical output low (sink) current characteristics.

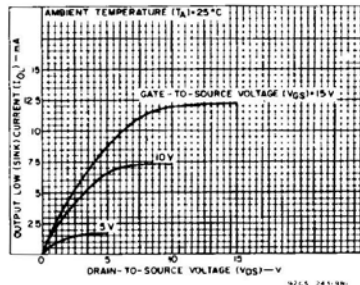


Fig. 2 — Minimum output low (sink) current characteristics.

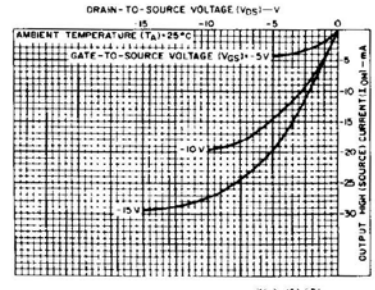


Fig. 3 — Typical output high (source) current characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Packages				+25			
				-55	-40	+85	+125	Min.	Typ.		Max.
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I _{IN} Max.		0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A=25°C; C_L=50 pF, Input t_r, t_f = 20 ns, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS V _{DD} VOLTS	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
Propagation Delay Time t _{PHL} , t _{PLH} E _I to E _O , E _I to G _S	5	110	220	
	10	55	110	
	15	45	85	
E _I to Q _M , D _n to G _S	5	170	340	ns
	10	85	170	
	15	65	125	
D _n to Q _M	5	220	440	
	10	110	220	
	15	85	160	
Transition Time t _{THL} , t _{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance C _{IN}	Any Input	5	7,5	μF

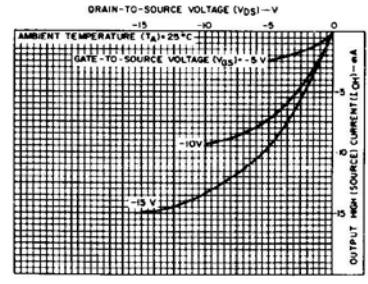


Fig. 4 - Minimum output high (source) current characteristics.

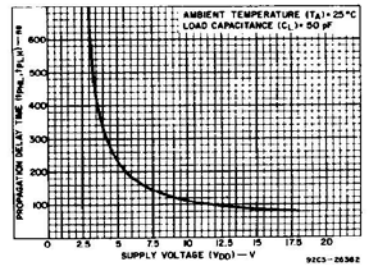


Fig. 5 - Typical propagation delay (D_n to Q_m) vs. supply voltage.

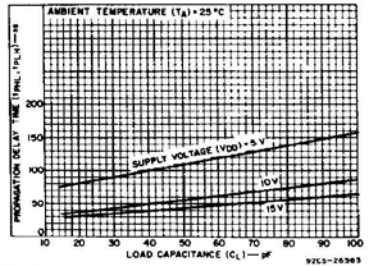


Fig. 6 - Typical propagation delay (E_I to G_S, E_I to E_O) vs. load capacitance.

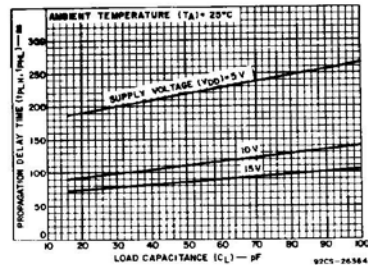
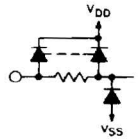
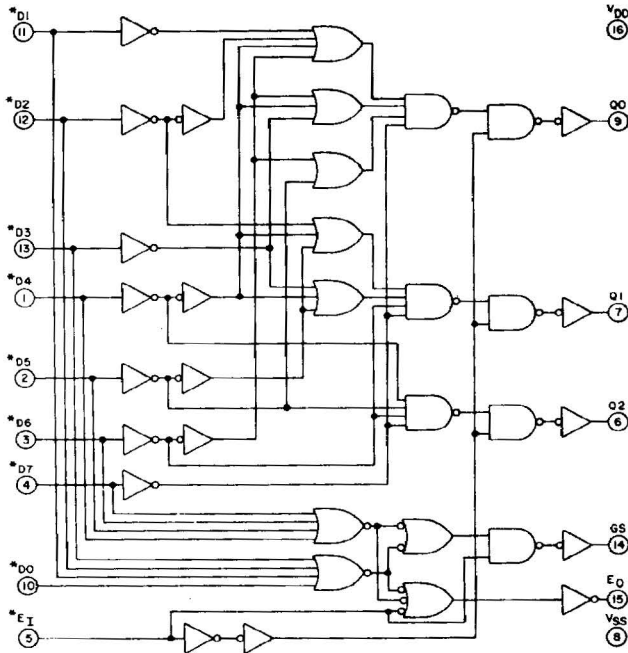


Fig. 7 - Typical propagation delay (D_n to Q_m) vs. load capacitance.

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*ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 8 - CD4532 logic diagram.

TRUTH TABLE

Input									Output				
E ₁	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	GS	Q ₂	Q ₁	Q ₀	E ₀
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Logic 1 ≡ High

Logic 0 ≡ Low

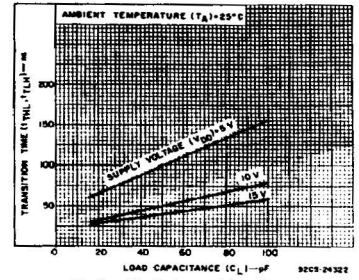


Fig. 9 - Typical transition time vs. load capacitance.

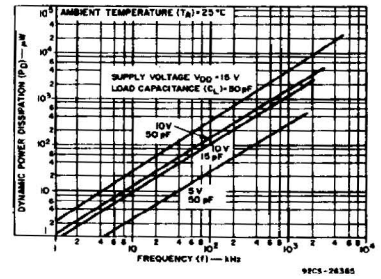


Fig. 10 - Typical dynamic power dissipation vs. frequency.

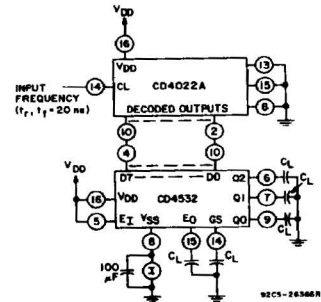


Fig. 11 - Dynamic power dissipation test circuit.

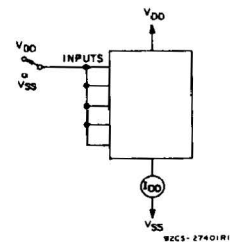


Fig. 12 - Quiescent device current test circuit.

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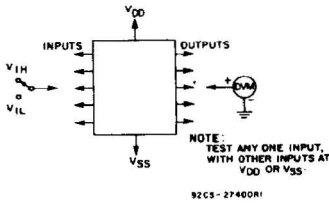


Fig. 13 - Input voltage test circuit.

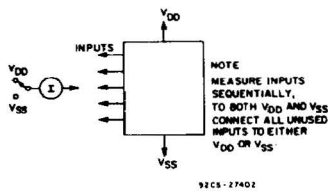
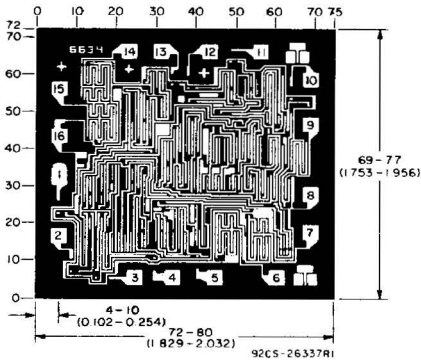


Fig. 14 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.

Dimensions and pad layout for CD4532BH.

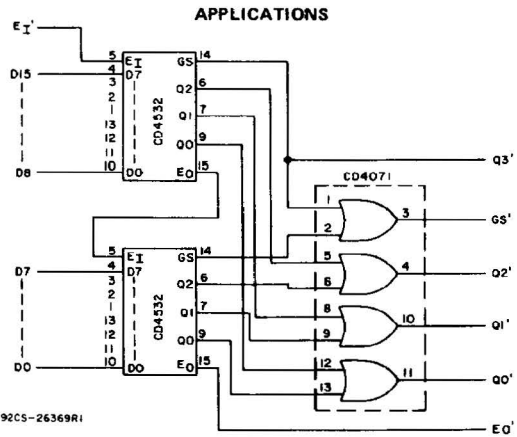
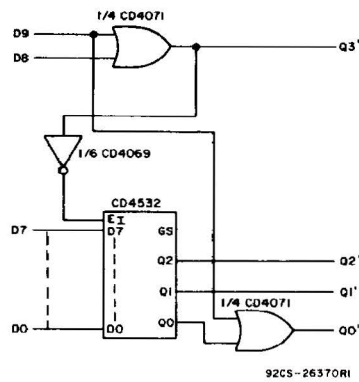


Fig. 15 - 16-level priority encoder.



TRUTH TABLE

Input										Output				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	0	1
0	0	0	0	1	X	X	X	X	X	1	0	1	0	0
0	0	0	0	0	1	X	X	X	X	1	0	0	1	1
0	0	0	0	0	0	1	X	X	X	1	0	0	1	0
0	0	0	0	0	0	0	1	X	X	1	0	0	0	1
0	0	0	0	0	0	0	0	1	X	1	0	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Logic 1 = High

Logic 0 = Low

Fig. 16 - 0-to-9 keyboard encoder.