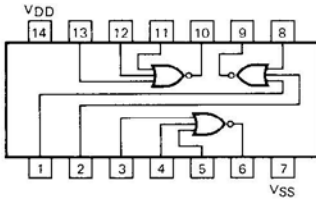


4025B

TRIPLE 3-INPUT NOR GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
I_{DD}	Quiescent Power	XC	1			2			4			μ A	MIN, 25°C	All inputs at 0 V or V_{DD}
			7.5			15			30				MAX	
	Supply Current	XM	0.25			0.5			1			μ A	MIN, 25°C	
			7.5			15			30				MAX	

AC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay	45			20			15			ns	$C_L = 50$ pF, $R_L = 200$ k Ω
t_{PHL}		110			60			48				
t_{TLH}	Output Transition Time	38			20			15			ns	Input Transition Times ≤ 20 ns
t_{THL}		135			70			45				

NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

