4019B
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The 4019B provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (Z_n) is the logical OR of the A_n and B_n inputs ($Z_n = A_n + B_n$). When S_A and S_B are LOW, output (Z_n) is LOW independent of the multiplexer inputs (A_n and B_n). The 4019B cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

PIN NAMES

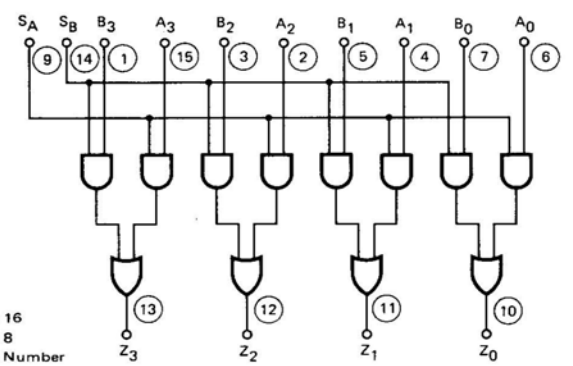
S_A, S_B	Select Inputs (Active HIGH)
$A_0 - A_3$, $B_0 - B_3$	Multiplexer Inputs
$Z_0 - Z_3$	Multiplexer Outputs

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

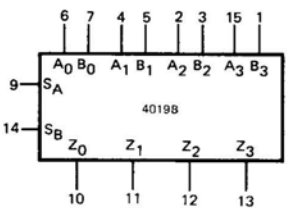
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

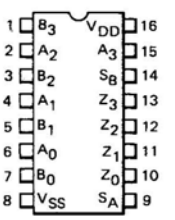
$Z_n = S_A A_n + S_B B_n$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	μA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600	μA	MIN, 25°C MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		75	150		35	70		24	56	ns	C_L = 50 pF,
t_{PHL}	S_A, S_B, A_n or B_n to Z_n		85	160		37	75		29	60	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		80	135		42	70		32	45	ns	Input Transition
t_{THL}			90	135		40	70		30	45	ns	Times ⩽ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

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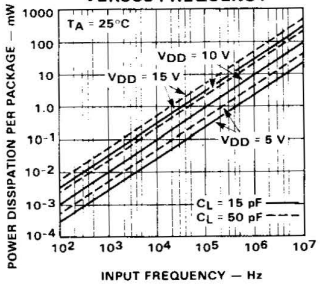
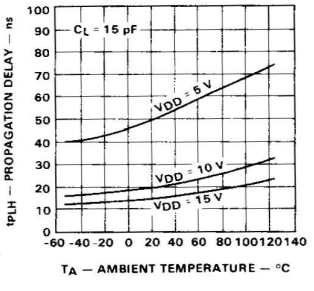
TYPICAL ELECTRICAL CHARACTERISTICS

POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE