

4014B

8-BIT SHIFT REGISTER

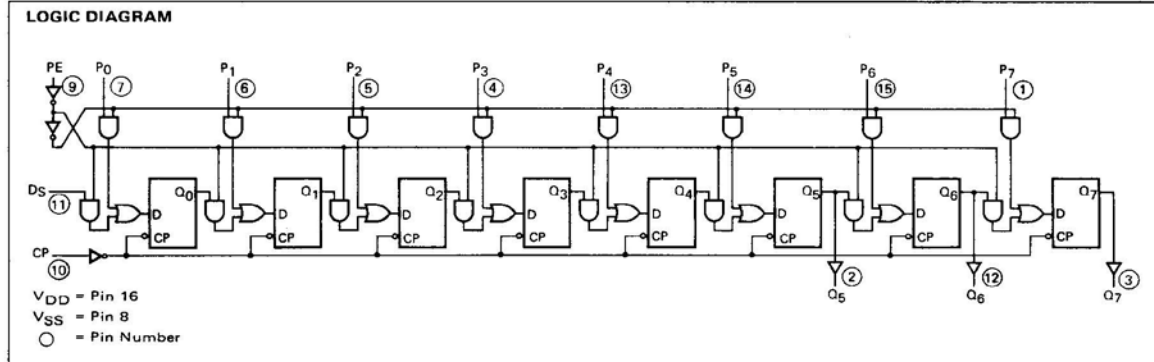
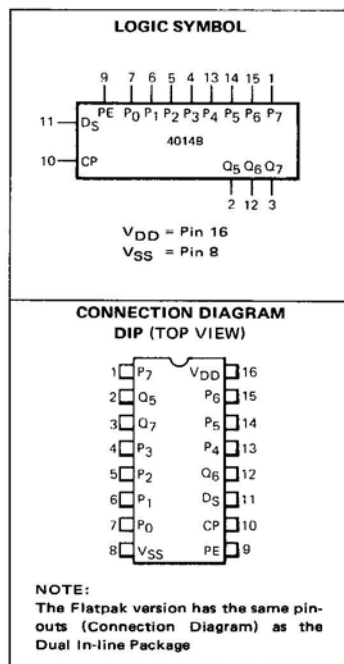
DESCRIPTION – The 4014B is a fully synchronous edge-triggered 8-Bit Shift Register with eight synchronous Parallel Inputs (P_0 - P_7), a synchronous Serial Data Input (D_S), a synchronous Parallel Enable Input (PE), a LOW-to-HIGH edge-triggered Clock Input (CP) and Buffered Parallel Outputs from the last three stages (Q_5 - Q_7).

Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from the Parallel Inputs (P_0 - P_7) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Input (D_S) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- TYPICAL SHIFT FREQUENCY OF 14.7 MHz AT $V_{DD} = 10$ V
- PARALLEL OR SERIAL TO SERIAL DATA TRANSFER
- AVAILABLE OUTPUTS FROM THE LAST THREE STAGES
- FULLY SYNCHRONOUS

PIN NAMES

PE	Parallel Enable Input
P_0 - P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5, Q_6, Q_7	Buffered Parallel Outputs from the Last Three Stages



FAIRCHILD CMOS • 4014B

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μ A	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
	XM			5			10			20	μ A	MIN, 25°C		
				150			300			600		MAX		

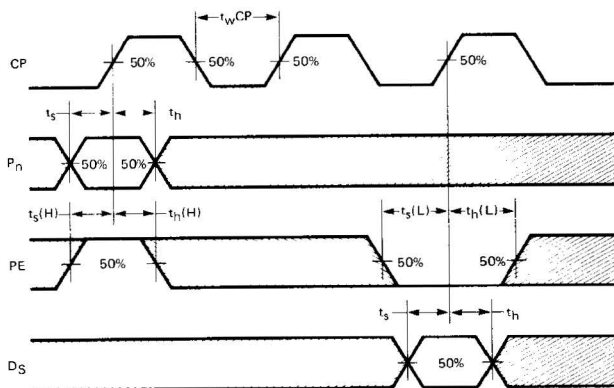
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to any Q		129	275		57	120		41	96	ns	$C_L = 50$ pF, $R_L = 200$ k Ω Input Transition Times < 20 ns
t_{PHL}			165	350		68	120		47	96	ns	
t_{TLH}	Output Transition Time		70	135		37	75		21	45	ns	
t_{THL}			77	135		34	75		21	45	ns	
t_{wCP}	CP Minimum Pulse Width	200	93		100	33		80	22		ns	
t_s	Set-Up Time PE to CP	300	118		80	44		64	29		ns	
t_h	Hold Time PE to CP	25	15		5	3		4	2		ns	
t_s	Set-Up Time D_S to CP	200	80		50	28		40	17		ns	
t_h	Hold Time D_S to CP	10	5		0	-1		0	-1		ns	
t_s	Set-Up Time P_n to CP	250	108		100	37		80	23		ns	
t_h	Hold Time P_n to CP	20	10		5	3		4	2		ns	
f_{MAX}	Max. Input Clock Frequency (Note 3)	2	5.8		5	14.7		6	17		MHZ	

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX} , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μ s at $V_{DD} = 5$ V, 4 μ s at $V_{DD} = 10$ V, and 3 μ s at $V_{DD} = 15$ V.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, D_S TO CP, AND P_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS

