File Number **1594**

2N6796

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

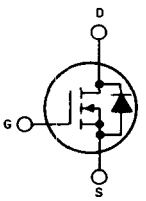
8.0A, 100V

$r_{DS}(on) = 0.18\ \Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

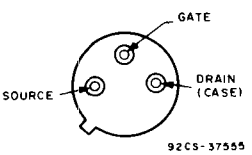
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

Absolute Maximum Ratings

Parameter		2N6796	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	A
I_{DM}	Pulsed Drain Current ③	32*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	8.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	32*	A
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.20* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6796

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		–	–	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	*Diode Forward Voltage* ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(℧)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	*Turn-On Delay Time*	–	–	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_o = 50Ω
t_r	Rise Time	–	–	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	45*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	*Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.*		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

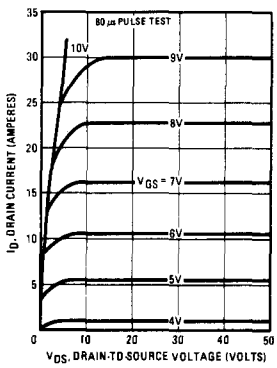


Fig. 1 – Typical Output Characteristics

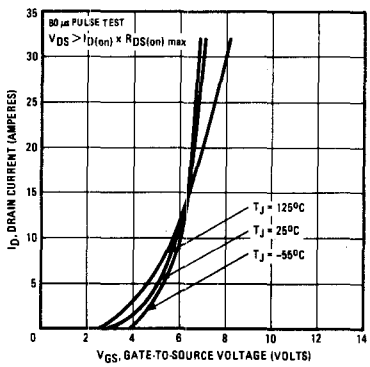


Fig. 2 – Typical Transfer Characteristics

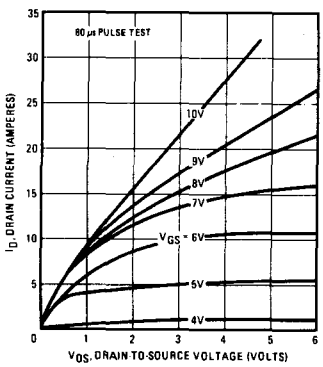


Fig. 3 – Typical Saturation Characteristics

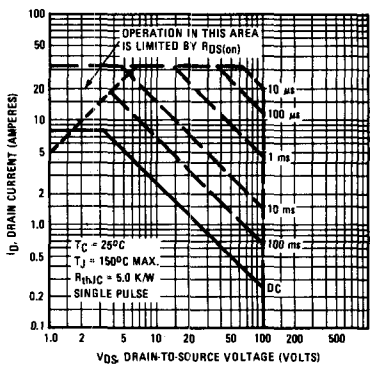


Fig. 4 – Maximum Safe Operating Area

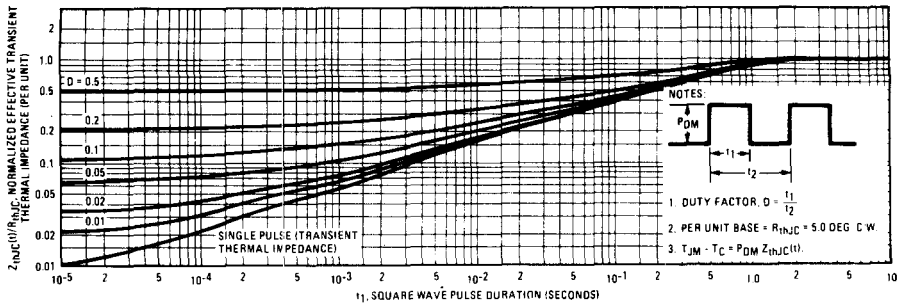


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

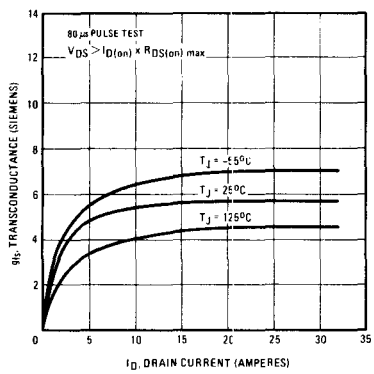


Fig. 6 – Typical Transconductance Vs. Drain Current

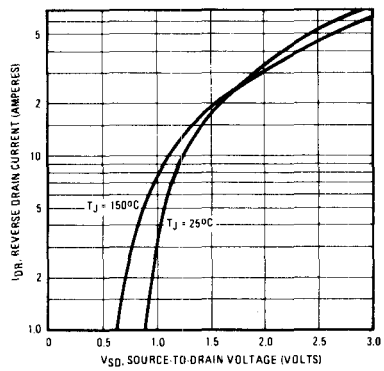


Fig. 7 – Typical Source-Drain Diode Forward Voltage

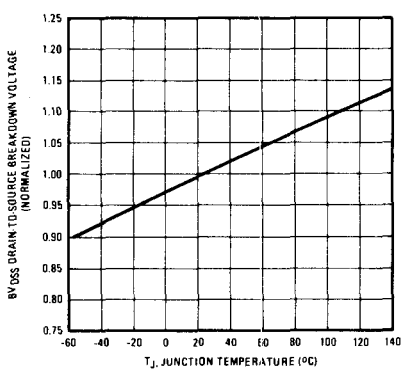


Fig. 8 – Breakdown Voltage Vs. Temperature

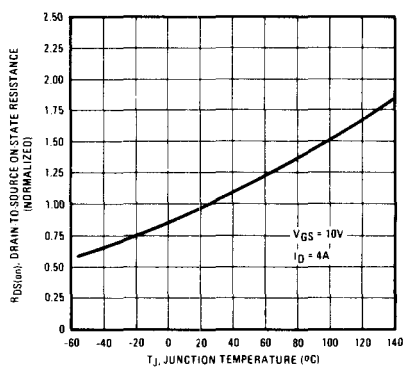


Fig. 9 – Normalized On-Resistance Vs. Temperature

2N6796

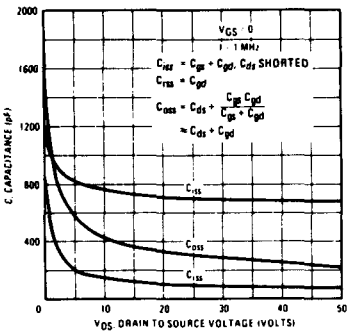


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

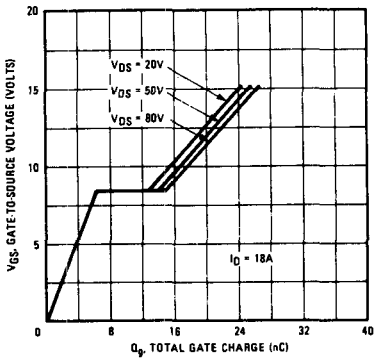


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

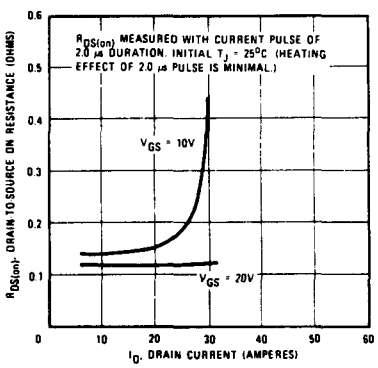


Fig. 12 – Typical On-Resistance Vs. Drain Current

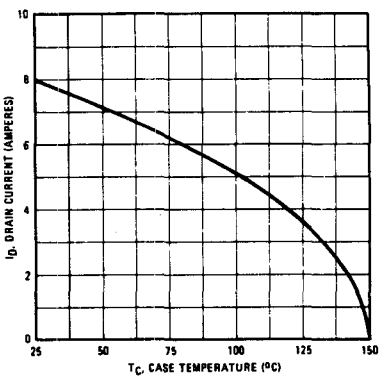


Fig. 13 – Maximum Drain Current Vs. Case Temperature

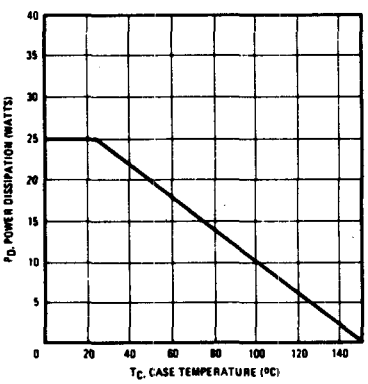
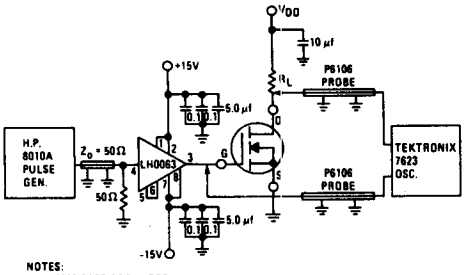
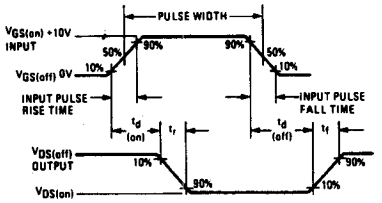


Fig. 14 – Power Vs. Temperature Derating Curve

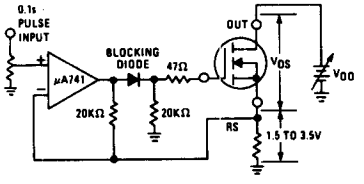


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S$ = 2.5 ± 1.0 Vdc.

Fig. 16 — Safe Operating Area Test Circuit

JAN, JANTX, and JANTXV

JAN, JANTX, and JANTXV Solid-State Power Devices

The major military specification used for the procurement of standard solid-state devices by the military is MIL-S-19500, which covers the devices such as discrete transistors, thyristors, and diodes.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).

Levels of reliability are defined by MIL-S-19500. JAN types receive Group A, Group B, and Group C lot sampling only, and are the least expensive. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot rejection based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types and types that are process of testing preliminary to QPL approval by DESC, respectively.

Custom high-reliability selections of Harris Power MOSFETs can also be supplied with similar process and power conditioning tests and delta criteria.

QPL Approved Types

Harris is presently qualified on the following devices. Prices and delivery quotations may be obtained from your local sales representative.

JAN and JANTX Power MOSFETs

N-Channel Types	MIL-S-19500/	Package	Channel	P_T (W)	I_D (A)	BV_{DSS} (V)	r_{DS} (on) Ω
2N6756	542	TO-204AA	N	75	14	100	0.18
2N6758	542	TO-204AA	N	75	9	200	0.4
2N6760	542	TO-204AA	N	75	5.5	400	1
2N6762	542	TO-204AA	N	75	4.5	500	1.5
2N6764	543	TO-204AE	N	150	38	100	0.055
2N6766	543	TO-204AE	N	150	30	200	0.085
2N6768	543	TO-204AA	N	150	14	400	0.3
2N6770	543	TO-204AA	N	150	12	500	0.4
2N6782	556	TO-205AF	N	15	3.5	100	0.6
2N6784	556	TO-205AF	N	15	2.25	200	1.5
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6790	555	TO-205AF	N	20	3.5	200	0.8
2N6792	555	TO-205AF	N	20	2	400	1.8
2N6794	555	TO-205AF	N	20	1.5	500	3
2N6796	557	TO-205AF	N	25	8	100	0.18
2N6798	557	TO-205AF	N	25	5.5	100	0.4
2N6800	557	TO-205AF	N	25	3	400	1
2N6802	557	TO-205AF	N	25	2.5	500	1.5
P-Channel Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6895	565	TO-205AF	P	8.33	-1.5	-100	3.65
2N6896	565	TO-204AA	P	60	-6	-100	0.6
2N6897	565	TO-204AA	P	100	-12	-100	0.3
2N6898	565	TO-204AA	P	150	-25	-100	0.2
2N6849	564	TO-205AF	P	25	-6.5	-100	0.3
2N6851	564	TO-205AF	P	25	-4.0	-200	0.8
N-Channel Logic-Level Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6901	566	TO-205AF	N	8.33	1.5	100	1.4
2N6902	566	TO-204AA	N	75	12	100	0.2
2N6903	566	TO-205AF	N	8.33	1.5	200	3.65
2N6904	566	TO-204AA	N	75	8	200	0.65