128-Mbit 1.8 Volt Intel® Wireless Flash Memory (W18) + 32-Mbit PSRAM Stacked-CSP Family

Datasheet

Product Features

- **Flash Architecture**
  - Flexible, Multiple-Partition, Dual-Operation: Read-While-Write / Read-While-Erase
  - 32 Partitions, 4 Mbits each
    - 31 Main Partitions, 8 Main Blocks each
    - 1 Parameter Partition, 8 Parameter + 7 Main Blocks
    - 32-Kword Main Blocks, 4-Kword Parameter Blocks
  - Single flash die- Top or Bottom Parameter
  - Dual flash die- Dual Parameter
- **Flash Performance**
  - 65 ns Initial Access Speed
  - 25 ns Async 4-Word Page-Mode Reads
  - 14 ns Sync Burst-Read Speed
  - 4-, 8-, 16-, Continuous-Word Burst Lengths
  - Burst-/ Page-Mode Reads in all Blocks and across all partition boundaries
  - Burst Suspend
  - Programmable WAIT Configuration
  - Enhanced Factory Programming Mode: 3.1µs/Word
  - Flash Protection Register
    - 64 Unique Device Identifier Bits
    - 64 User-Programmable OTP Bits
- **Flash Automation Suspend Operations**
  - Erase Suspend to Program or Read
  - Program Suspend to Read
  - 5µs (typ) Program/Erase Suspend Latency
- **Flash Software**
  - Intel® Flash Data Integrator (FDI) Optimized
  - Common Flash Interface (CFI)
- **Flash Data Protection**
  - Absolute Protection with VPP and WP#
  - Individual Dynamic Zero-Latency Block Locking
  - Individual Block Lock-Down
  - Erase/Program Lockout during Power Transitions
- **Stacked-CSP Architecture**
  - Flash
  - Flash + Flash
  - Flash + PSRAM
  - Flash + Flash + PSRAM
  - Reduces Board Space Requirement
  - Simplifies PCB Design Complexity
  - Easy Migration to Future Stacked-CSP Devices
- **Stacked-CSP Voltage**
  - 1.7 V to 1.95 V V_{CC}
  - 1.7 V to 2.24 V V_{CCQ} (Flash only)
  - 1.8 V to 1.95 V V_{CCQ} (Flash + PSRAM)
- **Stacked-CSP Packaging**
  - 0.8 mm Ball-Pitch Intel® Stacked-CSP
  - Area: 8x10 mm, Height: 1.2mm and 1.4mm
  - 88-Ball (8 x 10 Matrix): 80 Active Balls with 2 Support Balls at Each Corner
- **PSRAM Architecture and Performance**
  - 1.8 V to 1.95 V P-V_{CC}
  - 85 ns Access Speed
  - 8-Word Page Read
  - 30 ns for Page Read Speed
  - Low Power Mode
- **Flash Quality and Reliability**
  - Extended Temperature: –25 °C to +85 °C
  - Minimum 100K Block Erase Cycles
  - 0.13 µm ETOX™ VIII Process

Versatile and compact Stacked Chip Scale Package (Stacked-CSP) solutions have been created by combining 128-Mbit 1.8 Volt Intel® Wireless Flash Memory (W18) with low-power 32-Mbit PSRAM. Ideal for high-performance, low-power, board-constrained memory applications, the W18 + 32-Mbit PSRAM Stacked-CSP family retains all of the features of the discrete 1.8 Volt Intel® Wireless Flash Memory (W18) device: flexible, multi-partition architecture for Read-While-Write / Read-While-Erase (RWW/RWE) dual operation and high performance asynchronous/ synchronous burst reads. Device upgrades and migrations are easy with a common package footprint and signal ballout for all Stacked-CSP combinations. Manufactured on Intel® 0.13 micron ETOX™ VIII process technology, W18 provides the highest levels of quality and reliability.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

252634-001
February 2003

Contents

Revision History

Date of Revision	Version	Description
02/12/03	-001	Initial Release, Stacked Chip Scale Package

1.0 Introduction

This document contains information pertaining to the 128-Mbit 1.8 Volt Intel® Wireless Flash Memory (W18) + 32-Mbit PSRAM Stacked-CSP family. The intent of this document is to provide information where this Stacked-CSP device differs from the discrete 1.8 Volt Intel® Wireless Flash Memory device. Refer to the latest revision *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for flash product details not included in this document.

1.1 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
CUI	Command User Interface
DU	Do Not Use
ETOX	EPROM Tunnel Oxide
k (noun)	1 thousand
Kb	1024 bits
KB	1024 bytes
Kword	1024 words
M (noun)	1 million
Mb	1,048,576 bits
MB	1,048,576 bytes
OTP	One Time Programmable
PLR	Protection Lock Register
PR	Protection Register
PRD	Protection Register Data
RCR	Read Configuration Register
RFU	Reserved for Future Use
Stacked-CSP	Stacked Chip Scale Package
SR	Status Register
SRD	Status Register Data
Word	16 bits

1.2 Conventions

Group Membership Brackets: Square brackets will be used to designate group membership or to define a group of signals with a similar function, such as A[21:1] and SR[4,1], for example.

VCC vs. V_{CC}: When referring to a signal or package-connection name, the notation used is VCC, etc. When referring to a timing or electrical level, the notation used is subscripted such as V_{CC}, etc.

Device: This term is used interchangeably throughout this document to denote either a particular die, or the combination of the triple-die.

CE#[2:1], OE#[2:1]: This is the method used to refer to more than one chip-enable or output enable at the same time. When each is referred to individually, the reference will be CE#1 and OE#1 (for die #1), and CE#2 and OE#2 (for die #2).

VCC, P-VCC, S-VCC: When referencing flash memory signals or timings, the notation used is VCC or $V_{CC,}$ respectively. When the reference is to PSRAM signals or timings, the notation is prefixed with "P-" (e.g., P-VCC, P-V_{CC}). When referencing SRAM signals or timings, the notation is prefixed with "S-" (e.g., S-VCC or S-V_{CC}).

R-OE#, R-LB#, R-UB#, R-WE#: Used to identify OE#, LB#, UB#, WE# RAM signals, and are usually shared between 1 or 2 RAM die.

2.0 Product Description

This section provides an overview of the features and capabilities of the 128-Mbit 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family.

2.1 Product Overview

The 128-Mbit 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family encompasses multiple flash memory + 32-Mbit PSRAM die combinations. Products range from a flash-only, single-die device to a triple-die, dual flash + 32-Mbit PSRAM device. The user can choose 32-Mbit PSRAM combined with one or two flash memory dies, all offered in the same package footprint and signal ballout.

Table 1 summarizes the 128-Mbit 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family offerings.

Table 1. Stacked-CSP Family Matrix

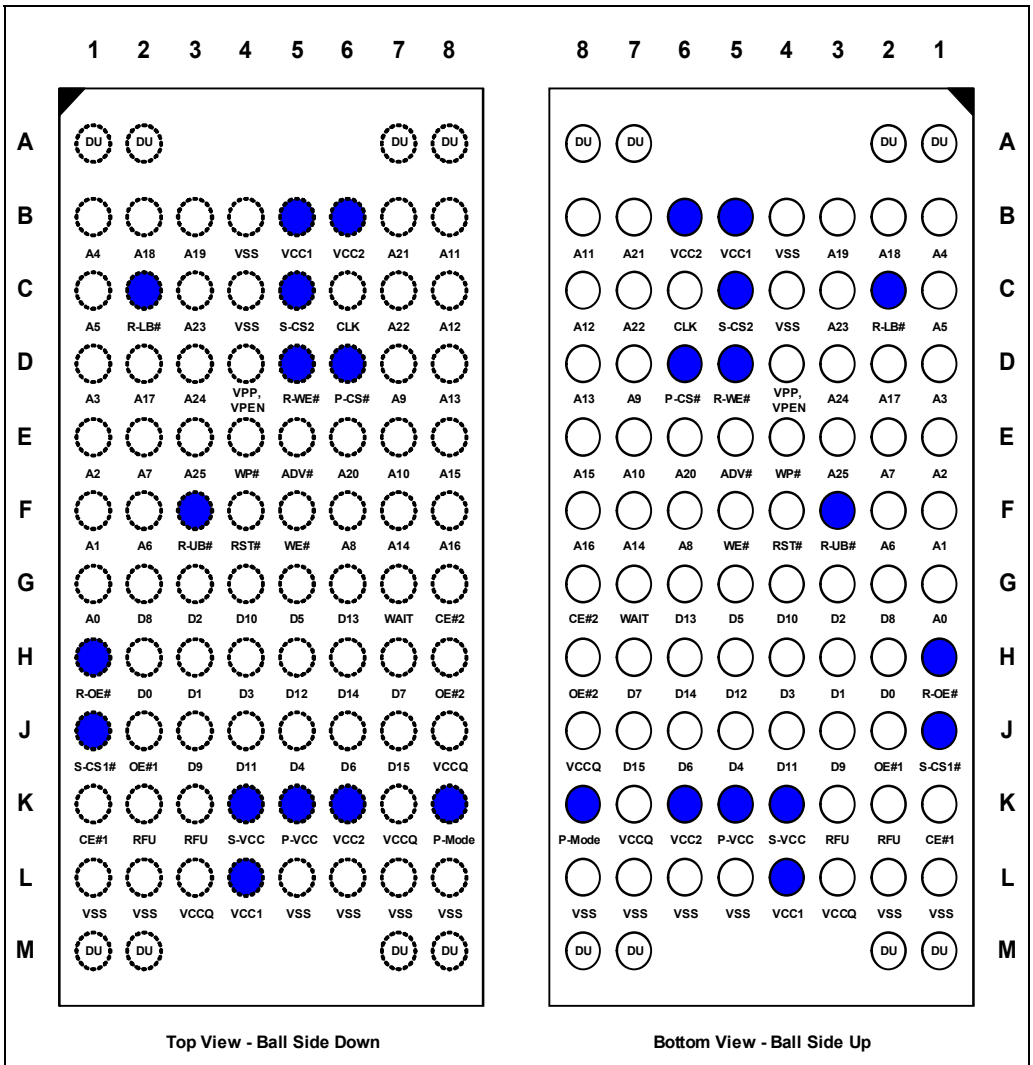
Line Item	Flash Die #1	Flash Die #2	RAM Die	Package Size (mm)	Notes
1	28F128W18T/B	None	None	8 x 10 x 1.2	1
2	28F128W18T/B	None	32M PSRAM	8 x 10 x 1.2	1
3	28F128W18B	28F640W18T	None	8 x 10 x 1.2	1,2
4	28F128W18B	28F640W18T	32M PSRAM	8 x 10 x 1.4	1,2
5	28F128W18B	28F128W18T	None	8 x 10 x 1.2	1,2
6	28F128W18B	28F128W18T	32M PSRAM	8 x 10 x 1.4	1,2

NOTES:
1. W18 = 1.8 Volt Intel® Wireless Flash Memory.
2. T/B = Top or Bottom boot; B = Bottom boot (flash die#1); T = Top boot (flash die#2)

2.2 Ballout Diagram

The 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family is available in an 88-ball (80-active ball) Stacked Chip-Scale Package (CSP) with a ball pitch of 0.8 mm. Figure 1 shows the ballout diagram for the 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family devices.

Figure 1. 88-Ball (80-Active Ball) Stacked-CSP Package Ballout



NOTE: Solid balls are shown as ballout differences between various stacked combinations across the Stacked-CSP Family. See Signal Descriptions for details on the electrical connections per stacked combination.

2.3 Signal Descriptions

Table 2 describes the active signals used on the 128-Mbit 1.8 Volt Intel® Wireless Flash Memory +32-Mbit PSRAM Stacked-CSP family.

Table 2. Signal Descriptions (Sheet 1 of 2)

Symbol	Type	Descriptions
A[Max:0]	Input	**ADDRESS INPUTS** for memory addresses of a SCSP device with: • 32-Mbit density: A[Max]=A20 • 64-Mbit density: A[Max]=A21 • 128-Mbit density: A[Max]=A22
D[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs data and commands during writing cycles, outputs data during memory, status register, protection register and configuration code reads. These signals float when the die or outputs are deselected. Data is internally latched during writes.
CE#1 CE#2	Input	**FLASH CHIP ENABLE:** CE#-low selects the flash component. When asserted, the flash internal control logic, input buffers, decoders, and sense amplifiers are activated. When deasserted, the flash die is deselected, power reduces to standby levels, and data and WAIT outputs are placed in high-Z state. CE#1 connects to flash die#1 Chip Enable while CE#2 connects to flash die#2 Chip Enable. CE#2 is only connected for stacked combinations with 2 flash dies.
RST#	Input	**FLASH RESET:** RST#-low resets flash internal circuitry and inhibits write operations. This function may be employed to provide data protection during power transitions. After exiting the reset state (RST# returned to logic-high), the selected flash die resumes operation in asynchronous read-array mode.
OE#1 OE#2	Input	**FLASH OUTPUT ENABLE:** OE#-low activates device output through the flash data buffers during a flash read cycle. When deasserted, the flash outputs tri-state to high-Z. OE#1 connects to flash die#1 Output Enable while OE#2 connects to flash die#2 Output Enable. OE#2 is only connected for stacked combinations with 2 flash dies.
WE#	Input	**FLASH WRITE ENABLE:** WE# controls writes to the selected flash die. WE#-low allows input to the flash CUI, array, PR/PLR, RCR, or block lock bits. Addresses and data are latched on this signal's rising edge.
ADV#	Input	**FLASH ADDRESS VALID:** ADV# indicates valid address presence on address inputs of the selected flash die. During synchronous read operations, all addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
CLK	Input	**FLASH CLOCK:** CLK synchronizes the selected flash die to the system bus frequency in synchronous-read configuration and increments an internal burst address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first. CLK is only used for synchronous mode. Refer to flash product discrete datasheet for information how to use this signal in asynchronous mode.
WAIT	Output	**FLASH WAIT:** Wait is driven when CE# is asserted. Flash RCR[10][WP] determines the WAIT asserted logic level. • In synchronous array read modes, WAIT indicates invalid data when asserted and valid data when de-asserted. • In synchronous non-array read modes, asynchronous page mode, and all write modes, WAIT is asserted. Refer to flash product discrete datasheet for more information.

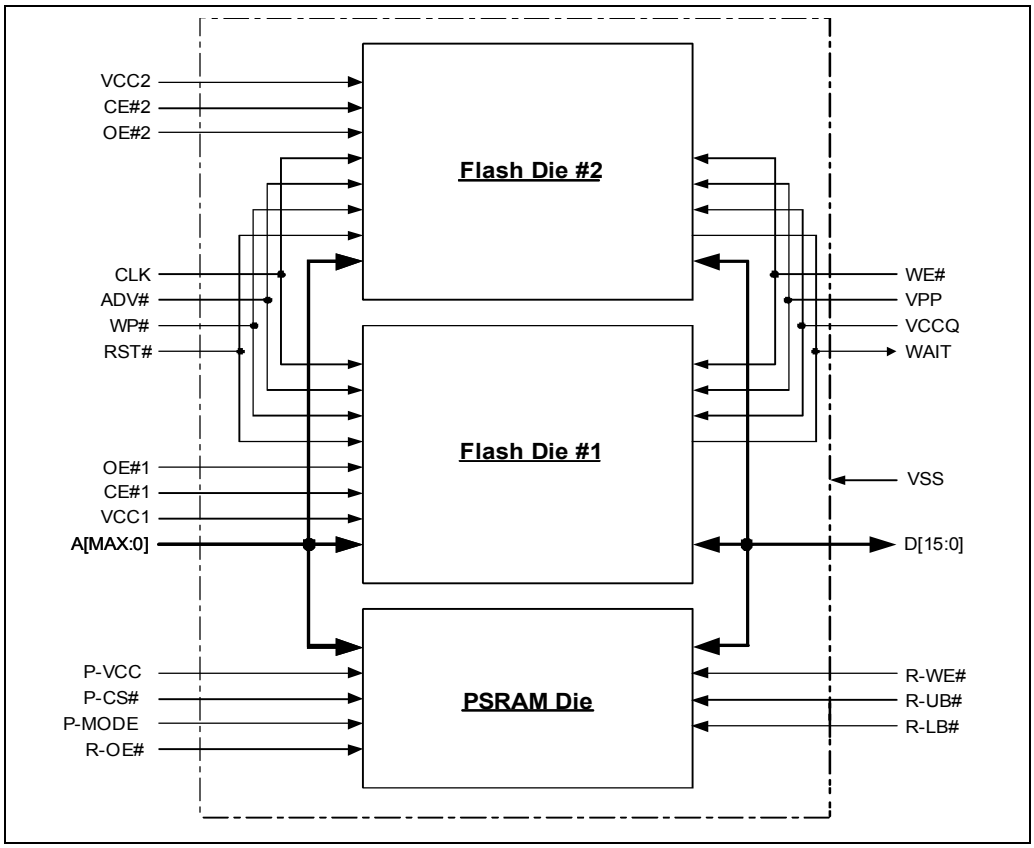
Table 2. Signal Descriptions (Sheet 2 of 2)

Symbol	Type	Descriptions
WP#	Input	**FLASH WRITE PROTECT:** Enables/disables the lock-down mechanism of the selected flash die. When WP# is logic low, the lock-down mechanism is enabled and blocks marked lock-down can not be unlocked through software.
VPP	Power	**FLASH PROGRAM / ERASE SUPPLY:** Valid Vpp voltage on this ball allow block erase and program functions. Flash memory array contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block Erase and program at invalid V_{PP} Voltage should not be attempted.
VCC1 VCC2	Power	**FLASH POWER SUPPLY:** Supplies power to the flash core. VCC1 connects to flash die#1 power supply while VCC2 connects to flash die#2 power supply. VCC2 is only connected for stacked combinations with 2 flash dies.
VCCQ	Power	**OUTPUT BUFFER POWER SUPPLY:** Supplies power for the input and output buffers.
VSS	Power	**GROUND:** Do not float any VSS connection.
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** Activates the SRAM internal control logic, input buffers, decoders, and sense amplifiers. When either are deasserted (S-CS1# = V_{IH} or S-CS2 = V_{IL}), the SRAM is deselected and its power reduces to standby levels. S-CS1# and S-CS2 are only connected for stacked combinations with SRAM die.
R-OE#	Input	**RAM OUTPUT ENABLE:** R-OE#-low activates device output through the selected RAM data buffers during a RAM read cycle. When deasserted, the selected RAM outputs tri-state to high-Z. R-OE# is only connected for stacked combinations with 1 or more RAM die.
R-WE#	Input	**RAM WRITE ENABLE:** R-WE#-low allows writes to the selected RAM array. R-WE# is only connected for stacked combinations with 1 or more RAM die.
R-UB# R-LB#	Input	**RAM UPPER / LOWER BYTE ENABLES:** R-UB#-low enables the selected RAM high-order bytes (D[15:8]). R-LB#-low enables the selected RAM low-order bytes (D[7:0]). R-UB# and R-LB# are only connected for stacked combinations with 1 or more RAM die.
S-VCC	Power	**SRAM POWER SUPPLY:** Supplies power for SRAM operations. S-VCC is only connected for stacked combinations with SRAM die.
P-CS#	Input	**PSRAM CHIP SELECT:** Activates the PSRAM internal control logic, input buffers, decoders, and sense amplifiers. When deasserted, the PSRAM is deselected and its power reduces to standby levels. P-CS# is only connected for stacked combinations with PSRAM die.
P-Mode	Input	**PSRAM REFRESH:** When deasserted, it enables PSRAM Lower Power Mode with partial array refresh or zero array refresh according to the Mode register setting. P-Mode is only connected for stacked combinations with PSRAM die.
P-VCC	Power	**PSRAM POWER SUPPLY:** Supplies power for PSRAM operations. P-VCC is only connected for stacked combinations with PSRAM die.
RFU		**RESERVED for FUTURE USE:** Do not drive RFU balls and leave them disconnected. Contact Intel regarding their future use.
DU		**DO NOT USE:** Do not connect to any other signal, or power supply; must be left floating.

2.4 Block Diagram

Figure 2 is a block diagram showing all internal package connections for the Stacked-CSP family with multiple dies. Refer to Table 1, "Stacked-CSP Family Matrix" on page 9 for valid combinations of flash and PSRAM die. Unused connections on combinations with less than triple die are reserved and should not be used.

Figure 2. Block Diagram



2.5 Flash Memory Map and Partitioning

Consult the latest *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for individual flash die memory map and partitioning information.

Refer to Table 1, "Stacked-CSP Family Matrix" on page 9 for valid configurations per stacked combination. Table 3 and Table 4 shows the Memory Map and Partitioning information for two flash memory die. Flash die#1(with CE#1 as its Chip Select) is configured to bottom boot while flash die#2(with CE#2 as its Chip Select) is configured to top boot.

Table 3. 128W18B+128W18T Dual-Flash Die SCSP Memory Map and Partitioning

Flash Die#	Partitioning		Block Size (KW)	Blk#	Address Range
Flash die #2(Top Boot) 128M-bit	Parameter Partition	One Partition	4	255-262	7F8000-7FFFFF
			32	248-254	7C0000-7F7FFF
	Main Partitions	One Partition	32	240-247	780000-7BFFFF
		One Partition	32	232-239	740000-77FFFF
		One Partition	32	224-231	700000-73FFFF
		Four Partitions	32	192-223	600000-6FFFFF
		Eight Partitions	32	128-191	400000-5FFFFF
		Sixteen Partitions	32	0-127	000000-3FFFFF
Flash die #1(Bottom Boot) 128-Mbit	Main Partitions	Sixteen Partitions	32	135-262	400000-7FFFFF
		Eight Partitions	32	71-134	200000-3FFFFF
		Four Partitions	32	39-70	100000-1FFFFF
		One Partition	32	31-38	0C0000-0FFFFF
		One Partition	32	23-30	080000-0BFFFF
		One Partition	32	15-22	040000-07FFFF
	Parameter Partition	One Partition	32	8-14	008000-03FFFF
			4	0-7	000000-007FFF

Table 4. 128W18B+64W18T Dual-Flash Die SCSP Memory Map and Partitioning

Flash Die#	Partitioning		Block Size (KW)	Blk #	Address Range
Flash die #2(Top Boot) 64-Mbit	Parameter Partition	One Partition	4	127-134	3F8000-3FFFFF
			32	120-126	3C0000-3F7FFF
	Main Partitions	One Partition	32	112-119	380000-3BFFFF
		One Partition	32	104-111	340000-37FFFF
		One Partition	32	96-103	300000-33FFFF
		Four Partitions	32	64-95	200000-2FFFFF
		Eight Partitions	32	0-63	000000-1FFFFF
Flash die #1(Bottom Boot) 128-Mbit	Main Partitions	Sixteen Partitions	32	135-262	400000-7FFFFF
		Eight Partitions	32	71-134	200000-3FFFFF
		Four Partitions	32	39-70	100000-1FFFFF
		One Partition	32	31-38	0C0000-0FFFFF
		One Partition	32	23-30	080000-0BFFFF
		One Partition	32	15-22	040000-07FFFF
	Parameter Partition	One Partition	32	8-14	008000-03FFFF
			4	0-7	000000-007FFF

3.0 Device Operation

3.1 Bus Operations

Bus operations for the 128-Mbit 1.8 Volt Intel® Wireless Flash Memory + 32-Mbit PSRAM Stacked-CSP family involve the multiple control chip enable (CE#1 for flash die#1 and CE#2 for flash die#2) and output enable (OE#1 for flash die#1 and OE#2 for flash die#2) signals. All other control signals are shared between the two flash die. Table 5 to Table 6 explains the bus operations of products across this SCSP family. Refer to the W18 datasheet (order number 290701) for single flash die SCSP bus operations.

Table 5. Flash Die#1 + Flash Die#2 Bus Operations

Device	Mode	RST#	CE#1	OE#1	WE#	ADV	VPP	WAIT	CE#2	OE#2	D[15:0]	Notes
Flash Die#1 Enabled	Sync Array Read	H	L	L	H	L	X	Active	H	X	Flash D_{OUT}	2,3,4
	All Async / Sync Non-Array Read	H	L	L	H	X	X	Asserted	H	X	Flash D_{OUT}	1,3,4,5
	Write	H	L	H	L	X	V_{PP1} or V_{PP2}	Asserted	H	X	Flash D_{IN}	3,4,6
	Output Disable	H	L	H	H	X	X	Active	X	X	Flash High-Z	4
	Standby	H	H	X	X	X	X	High-Z	X	X	Flash High-Z	4
	Reset	L	X	X	X	X	X	High-Z	X	X	Flash High-Z	4
Flash Die#2 Enabled	Sync Array Read	H	H	X	H	L	X	Active	L	L	Flash D_{OUT}	2,3,4
	All Async / Sync Non-Array Read	H	H	X	H	X	X	Asserted	L	L	Flash D_{OUT}	1,3,4,5
	Write	H	H	X	L	X	V_{PP1} or V_{PP2}	Asserted	L	H	Flash D_{IN}	3,4,6
	Output Disable	H	X	X	H	X	X	Active	L	H	Flash High-Z	4
	Standby	H	X	X	X	X	X	High-Z	H	X	Flash High-Z	4
	Reset	L	X	X	X	X	X	High-Z	X	X	Flash High-Z	4

NOTES:
1. For asynchronous read operation, both die may be simultaneously selected, but may not simultaneously drive the memory bus. See Section 3.2, “Flash Command Definitions” on page 17 for details regarding Flash selection overlap.
2. WAIT is only active during synchronous Flash reads. WAIT is driven if CE# is asserted. Refer to the 1.8-Volt Intel® Wireless Flash Memory datasheet (order number 290701) for further information regarding WAIT Signal.
3. For either Flash die, OE#1/OE#2 and WE# should never be asserted simultaneously. If done so on a particular flash die, OE#1/OE#2 will override WE#.
4. L means V_{IL} while H means V_{IH}. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
5. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
6. Refer to W18 datasheet for valid D_{IN} during Flash writes.

Table 6. Flash (Single Die/Dual Die) + PSRAM Bus Operations

Device	Mode	RST#	CE#X	OE#X	WE#	ADV#	VPP	WAIT	P-CS#	P-Mode	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
Flash Die(#1 or #2) Enabled	Sync Array Read	H	L	L	H	L	X	Active	PSRAM must be in High-Z					Flash D_{OUT}	1,2,3, 4,6
	All Async/ Sync Non-array Read	H	L	L	H	X	X	Asserted						Flash D_{OUT}	1,2,3, 4,6,7
	Write	H	L	H	L	L	V_{PP1} or V_{PP2}	Asserted						Flash D_{IN}	3,4,6, 8
	Output Disable	H	L	H	H	X	X	Active	Any PSRAM mode allowed					Flash High-Z	6
	Standby	H	H	X	X	X	X	High-Z						Flash High-Z	6
	Reset	L	X	X	X	X	X	High-Z						Flash High-Z	6
PSRAM Enabled	Read	Flash must be in High-Z						Note 2	L	H	L	H	L	PSRAM D_{OUT}	1,5
	Write								L	H	H	L	L	PSRAM D_{IN}	5
	Output Disable	Any flash mode allowed							L	H	H	H	X	PSRAM High-Z	6
	Standby								H	H	X	X	X	PSRAM High-Z	6
	Low Power Mode								X	L	X	X	X	PSRAM High-Z	6

NOTES:

1. For asynchronous read operation, all dies may be simultaneously selected, but may not simultaneously drive the memory bus. For synchronous burst-mode reads, only two die (one flash and the PSRAM) may be simultaneously selected.
2. WAIT is only valid during synchronous flash reads. Refer to the discrete datasheet for detailed Wait functionality.
3. CE#X is CE#1 for flash die#1, CE#2 for flash die#2. OE#X is OE#1 for flash die#1, OE#2 for flash die#2.
4. For either flash die, OE#X and WE# should never be asserted simultaneously. If done so on a particular flash die, OE#X will override WE#.
5. For PSRAM, R-OE# and R-WE# should never be asserted simultaneously.
6. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for V_{PP}.
7. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
8. Refer to W18 datasheet for valid D_{IN} during flash writes.

3.2 Flash Command Definitions

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Command Definitions.

4.0 Flash Read Operations

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Read Modes and Operations.

5.0 Flash Program Operations

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Program Operations.

6.0 Flash Erase Operations

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Erase Operations.

7.0 Flash Security Modes

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Security Modes and Operations.

8.0 Flash Read Configuration Register

Refer to the 1.8 Volt Intel® Wireless Flash Memory datasheet (order number 290701) for information regarding Flash Read Configuration Register (RCR) functions and programming.

9.0 Flash Power Consumption

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for information regarding Flash Power Considerations and Consumption.

10.0 Electrical Specifications

10.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 7. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded	–25	+85	°C	
Storage Temperature	–55	+125	°C	
Voltage On Any Signal (except V_{CC1}, V_{CC2}, V_{CCQ}, V_{PP}, and P-V_{CC})	–0.5	+2.45	V	1
V_{CC1} and V_{CC2} Voltage	–0.2	+2.45	V	1
V_{CCQ}, and P-V_{CC} Voltage	–0.2	+2.45	V	1
V_{PP} Voltage	–0.2	+14.0	V	1,2,3
Ish Output Short Circuit Current	–	100	mA	4

NOTES:
1. All Specified voltages are relative to V_{SS}. Minimum DC voltage is –0.5 V on input/output signals, –0.5 V on VCC and VPP signals. During transitions, this level may overshoot to –2.0 V for periods < 20 ns, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
2. Maximum DC voltage on VPP may overshoot to +14.0 V for periods < 20 ns.
3. V_{PP} program voltage is normally V_{PP1}. The maximum DC voltage on V_{PP} may overshoot to +14 V for periods < 20 ns. V_{PP} can be V_{PP2} for 1000 erase cycles on main blocks, 2500 cycles on parameter blocks.
4. Output shorted for no more than one second. No more than one output shorted at a time.

10.2 Operating Conditions

Table 8. Extended Temperature Operation

Symbol	Parameter	Flash/ Flash+Flash		Flash+PSRAM/ Flash+Flash+PSRAM		Unit
		Min	Max	Min	Max	
T_C	Operating Temperature	–40	+85	–25	+85	°C
V_{CC}	Flash Supply Voltage	1.7	1.95	1.7	1.95	V
V_{CCQ} $P\text{-}V_{CC}$	Flash I/O Voltage PSRAM Supply Voltage	1.7	2.24	1.8	1.95	V
V_{PP1}	Flash Program Logic Level	0.9	1.95	0.9	1.95	V
V_{PP2}	Flash Factory Program Voltage	11.4	12.6	11.4	12.6	V

NOTE: VPP is normally V_{PP1}. VPP can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles on parameter blocks at extended temperature.

10.3 Capacitance

NOTICE: Refer to the 1.8-Volt Intel® Wireless Flash Memory datasheet (order number 290701) for flash capacitance details. For SCSP products with two flash die, flash capacitances for each of the flash die need to be considered accordingly.

Table 9. PSRAM Capacitance

Symbol	Parameter	Max	Unit	Condition
C_{IN}	Input Capacitance	8	pF	T_C=25 °C, f=1MHz, V_{IN}=0V
$C_{I/O}$	Input/Output Capacitance	10	pF	

10.4 DC Characteristics

32-Mbit PSRAM DC characteristics are shown in Table 10. Refer to the 1.8 Volt Intel® Wireless Flash Memory datasheet (order number 290701) for Flash DC Characteristics.

NOTICE: DC Characteristics of all die in a SCSP device need to be considered accordingly, depending on the SCSP device operation.

Table 10. PSRAM DC Characteristics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
$P\text{-}V_{CC}$	Voltage Range			1.8	–	1.95	V
I_{CC}	Operating Current at Min cycle time	$I_{I/O}$=0mA		–	–	35	mA
I_{SB1}	Standby Current	P-CS#≥P-V_{CC}-0.2V, P-Mode ≥ P-V_{CC}-0.2V		–	90	100	µA
I_{SB2}	Low Power Mode	P-CS#≥P-V_{CC}-0.2V, P-Mode≤0.2V	16 Mbits	–	60	70	
			8 Mbits	–	50	60	
			4 Mbits	–	40	50	
			0 Mbits	–	20	30	
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA		0.8P-Vcc	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		–	–	0.2P-Vcc	V
V_{IH}	Input High Voltage			0.8P-Vcc	–	P-V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3	–	0.2P-V_{CC}	V
*I_{IL}	Input Leakage Current	V_{IN}=0V to P-Vcc		–1.0	–	+1.0	µA
*I_{OL}	Input/Output Leakage Current	$V_{I/O}$=0V to P-Vcc, P-CS#=V_{IH} or R-WE#=V_{IH} or R-OE#=V_{IH}		–1.0	–	+1.0	

* V_{IN}: Input voltage, $V_{I/O}$: Input/Output voltage

11.0 AC Characteristics

11.1 Flash AC Characteristics

Refer to the 1.8-Volt Intel® Wireless Flash Memory datasheet (order number 290701) for Flash AC Characteristics details not included in Table 11 below.

Table 11. Flash AC Read Characteristics

Sym	Parameter	128W18		64W18		Unit
		Min	Max	Min	Max	
Asynchronous Specifications						
t_{AVAV}	Read Cycle Time	65		65		ns
t_{AVQV}	Address to Output Delay		65		65	ns
t_{ELQV}	CE# Low to Output Delay		65		65	ns
t_{VLQV}	ADV# Low to Output Delay		65		65	ns
Latching Specifications						
t_{APA}	Page Address Access Time		25		25	ns
Clock Specifications						
t_{CHQV}	CLK to Output Delay		14		14	ns

11.2 PSRAM AC Characteristics

Table 12. PSRAM AC Characteristics—Read-Only Operations

#	Symbol	Parameter	32M		Unit	Note
			Min	Max		
Read Cycle						
R1	t_{RC}	Read Cycle Time	85	–	ns	
R2	t_{AA}	Address access time	–	85	ns	
R3	t_{CO}	P-CS# Low to Output Valid	–	85	ns	
R4	t_{OE}	R-OE# Low to Output Valid	–	65	ns	
R5	t_{BA}	R-UB#, R-LB# Low to Output Valid	–	85	ns	
R6	t_{LZ}	P-CS# Low to Output in Low-Z	10	–	ns	
R7	t_{OLZ}	R-OE# Low to Output in Low-Z	5	–	ns	
R8	t_{HZ}	P-CS# High to Output in High-Z	–	25	ns	
R9	t_{OHZ}	R-OE# High to Output in High-Z	–	25	ns	
R10	t_{OH}	Output Hold from Address change	5	–	ns	
R11	t_{BLZ}	R-UB#, R-LB# Low to Output in Low-Z	5	–	ns	
R12	t_{BHZ}	R-UB#, R-LB# High to Output in High-Z	–	25	ns	
R13	t_{ASO}	Address set to R-OE# low level	0	–	ns	1
R14	t_{OHAH}	R-OE# high level to address hold	-5	–	ns	
R15	t_{CHAH}	P-CS# high level to address hold	0	–	ns	1
R16	t_{BHAH}	R-LB#, R-UB# high level to address hold	0	–	ns	1,2
R17	t_{CLOL}	P-CS# low level to R-OE# low level	0	10,000	ns	3
R18	t_{OLCH}	R-OE# low level to P-CS# high level	60	–	ns	
R19	t_{CP}	P-CS# high level pulse width	10	–	ns	
R20	t_{BP}	R-UB#, R-LB# high level pulse width	10	–	ns	
R21	t_{OP}	R-OE# high level pulse width	–	10,000	ns	3
Page Mode						
PR1	t_{PC}	Page Cycle Time	30	–	ns	4
PR2	t_{PA}	Page Mode Address Access Time	–	30	ns	

NOTE:
1. When R13≥\|R15\|, \|R16\|. The minimum of R15 and R16 are -15 ns. (See Figure 3, “Conditions for Calculating R15 and R16 Minimum Values” on page 22.)
2. R16 is specified from when both R-LB# and R-UB# become high level.
3. R17 and R21(MAX) are applied while P-CS# is being hold at low level.
4. See Figure 5, “AC Waveform of PSRAM Read Operations” on page 24.

Figure 3. Conditions for Calculating R15 and R16 Minimum Values

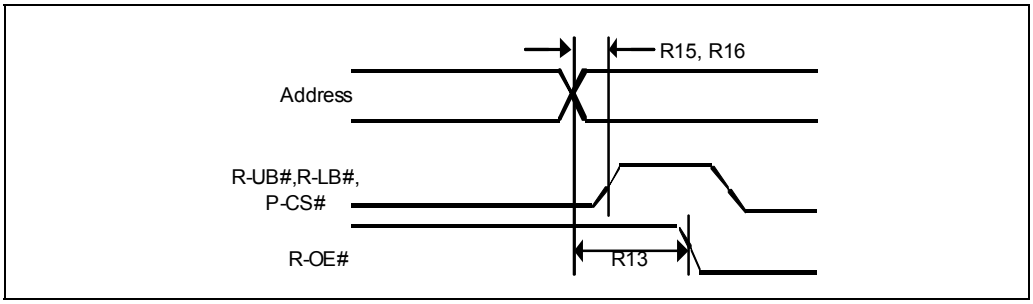


Table 13. PSRAM AC Characteristics—Write Operations

#	Symbol	Parameter	32M		Unit	Note
			Min	Max		
W1	t_{WC}	Write Cycle Time	85	–	ns	
W2	t_{AS}	Address Setup Time	0	–	ns	
W3	t_{WP}	Write Pulse Width	60	–	ns	
W4	t_{DW}	Data valid to Write End	30	–	ns	
W5	t_{AW}	Address valid to end of write	70	–	ns	
W6	t_{CW}	P-CS# to end of write	70	–	ns	
W7	t_{DH}	Data Hold time	0	–	ns	
W8	t_{WR}	Write Recovery	0	–	ns	
W9	t_{BW}	R-UB#, R-LB# Setup to end of Write	70	–	ns	
W10	t_{CP}	P-CS# High level pulse width	10	–	ns	
W11	t_{BP}	R-UB#, R-LB# High level pulse width	10	–	ns	
W12	t_{WHP}	R-WE# High level pulse width	10	–	ns	
W13	t_{OHAH}	R-OE# High level to address hold	-5	–	ns	
W14	t_{CHAH}	P-CS# High level to address hold	0	–	ns	1
W15	t_{BHAH}	R-UB#, R-LB# High level to address hold	0	–	ns	1,2
W16	t_{OES}	R-OE# High level to R-WE# set	0	10,000	ns	3
W17	t_{OEH}	R-WE# High level to R-OE# set	10	10,000	ns	

NOTES:
1. When W2 ≥|W14|, |W15| and W10≥18ns, W14 and W15 (MIN) are -15 ns. (See Figure 4, “Conditions for Calculating W14 and W15 Minimum Values” on page 23.)
2. W15 is specified from when both R-LB# and R-UB# become high level.
3. W16 and W17(MAX) are applied while P-CS# is being hold at low level.
4. See Figure 7, “AC Waveform PSRAM Write Operation” .

Figure 4. Conditions for Calculating W14 and W15 Minimum Values

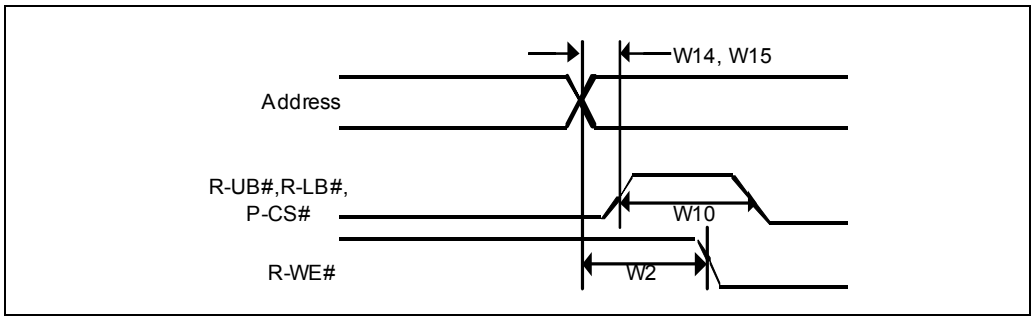
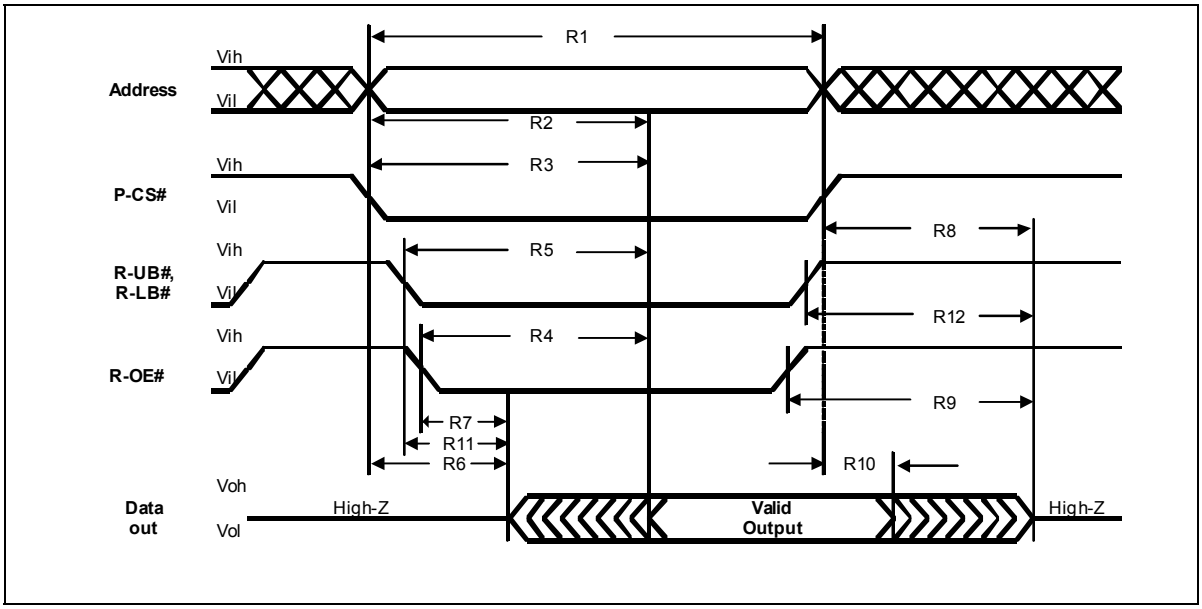
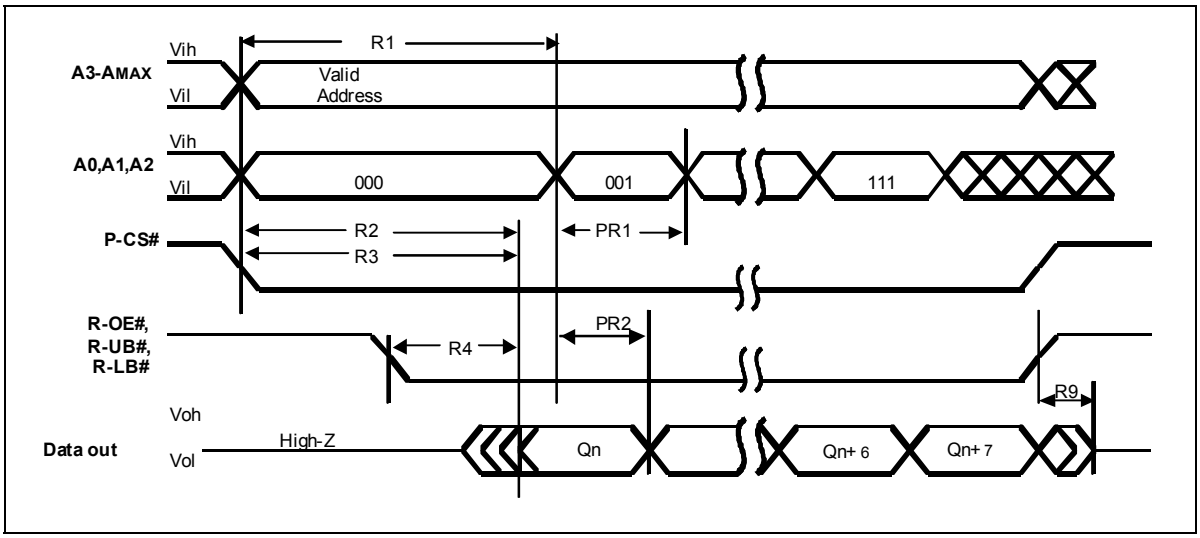


Figure 5. AC Waveform of PSRAM Read Operations



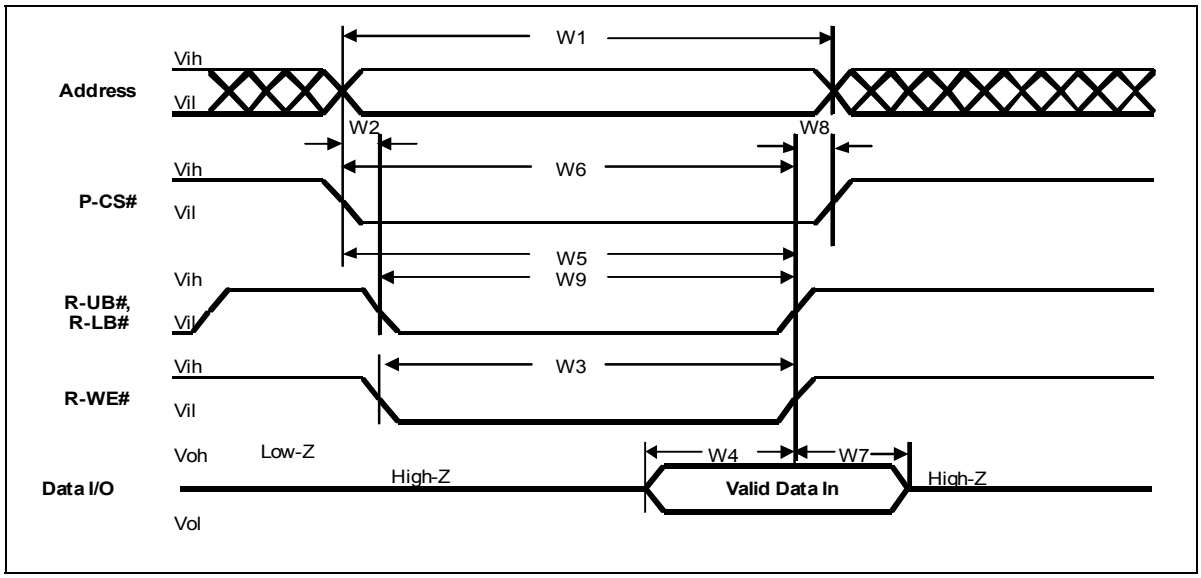
NOTE: In read cycle, P-Mode and R-WE# should be fixed to high level

Figure 6. AC Waveform of PSRAM 8-Word Page Read Operation



NOTE: In page read cycle, P-Mode and R-WE# should be fixed to high level, and R-UB#, R-LB# are low level.

Figure 7. AC Waveform PSRAM Write Operation



NOTES:

1. During address transition, at least one of pins P-CS#, R-WE#, or both of R-UB# and R-LB# pins should be inactivated.
2. Do not input data to the I/O pins while they are in the output state.
3. In write cycle, P-Mode and R-OE# should be fixed to high level.
4. Write operation is done during the overlap time of a low level P-CS#, R-WE#, R-LB# and/or R-UB#.

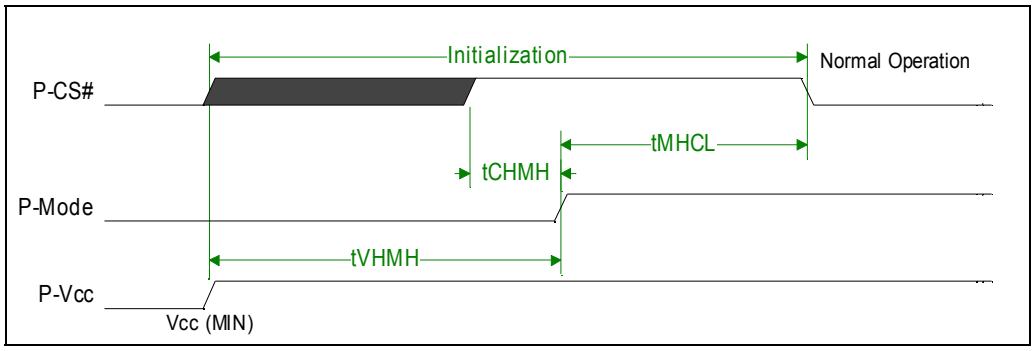
12.0 PSRAM Operations

12.1 Power-up Sequence and Initialization

The PSRAM functionality and reliability are independent of the power-up slew rate of the core P-V_{CC}. Any power-up slew rate is possible under use conditions.

The following power up sequence and operation should be used before starting normal operation. The PSRAM power-up sequence is represented in Figure 8. Following power application, make P-Mode high level after fixing P-Mode to low level for the period of t_{VHMH}. Make P-CS# high level before making P-Mode high level. Then, P-CS# and P-Mode are fixed to high level for the period of t_{MHCL}. Normal Operation is possible once the power up sequence is complete.

Figure 8. Timing Waveform for Power up sequence



NOTES:
1. Make P-Mode low level when starting the power supply.
2. t_{VHMH} is specified from when the power supply voltage reaches the prescribed minimum value (P-Vcc (MIN))

Table 14. Initialization timing

Parameter	Symbol	MIN	MAX	Unit
Power application to P-Mode low level hold	t_{VHMH}	50		us
P-CS# high level to P-Mode high level	t_{CHMH}	0		ns
Following power application, P-Mode high level hold to P-CS# low level	t_{MHCL}	200		us

12.2 Mode Register

The PSRAM die has an internal register that helps control the Low Power mode of the PSRAM. This register is called the Mode register. The densities that can be selected for performing refresh are 16 Mbits, 8 Mbits, 4 Mbits and 0 Mbit. The density for performing refresh can be set with the Mode register. Once the refresh density has been set in the Mode register, these settings are retained until they are set again, while applying the power supply. However, the Mode register setting will become undefined if the power is turned off, so set the Mode register again after power application.

12.2.1 Mode Register Setting

Since the initial value of the Mode register at power application is undefined, be sure to set the Mode register after initialization at power application. When setting the density of partial refresh, data before entering the Low Power Mode is not guaranteed.(This is the same for resetup) However, since Low Power Mode is not entered unless P-Mode=L, when partial refresh is not used, it is not necessary to set the Mode register. Moreover, when using page read without using partial refresh, it is not necessary to set the Mode register.

The Mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address. The Mode register setting is a continuous four-cycle operation - two read cycles and two writes cycles. See Table 15 for setting Mode register command sequence.

Table 15. Setting Mode Register Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
Partial refresh density	Address	Data	Address	Data	Address	Data	Address	Data
16 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	04H
8 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	05H
4 Mbits	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	06H
0 Mbit	Highest Address	–	Highest Address	–	Highest Address	00H	Highest Address	07H

For the timing chart and flow chart, refer to Figure 9 and Figure 10.

Figure 9. Mode Register Update--Timing Waveform

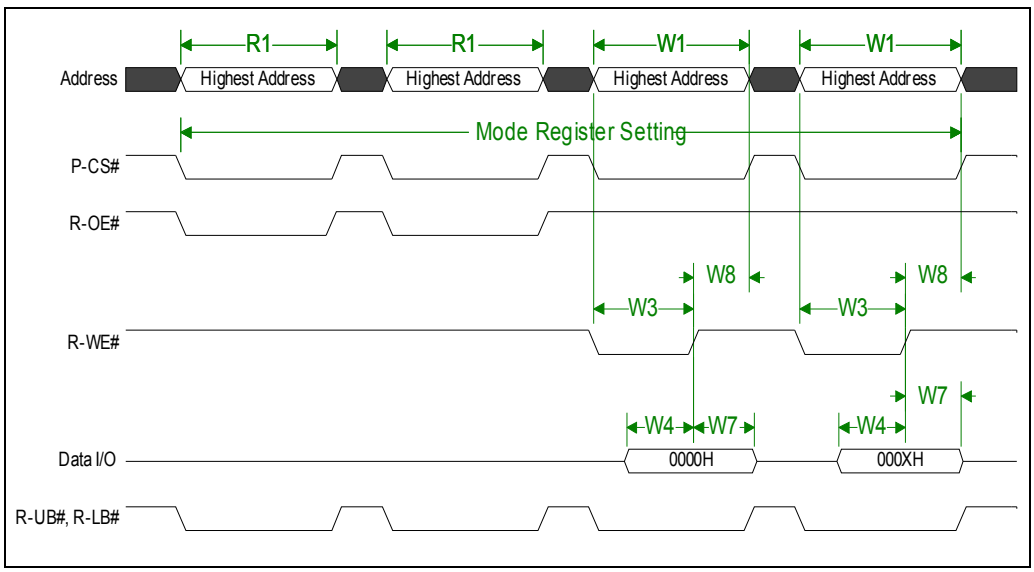
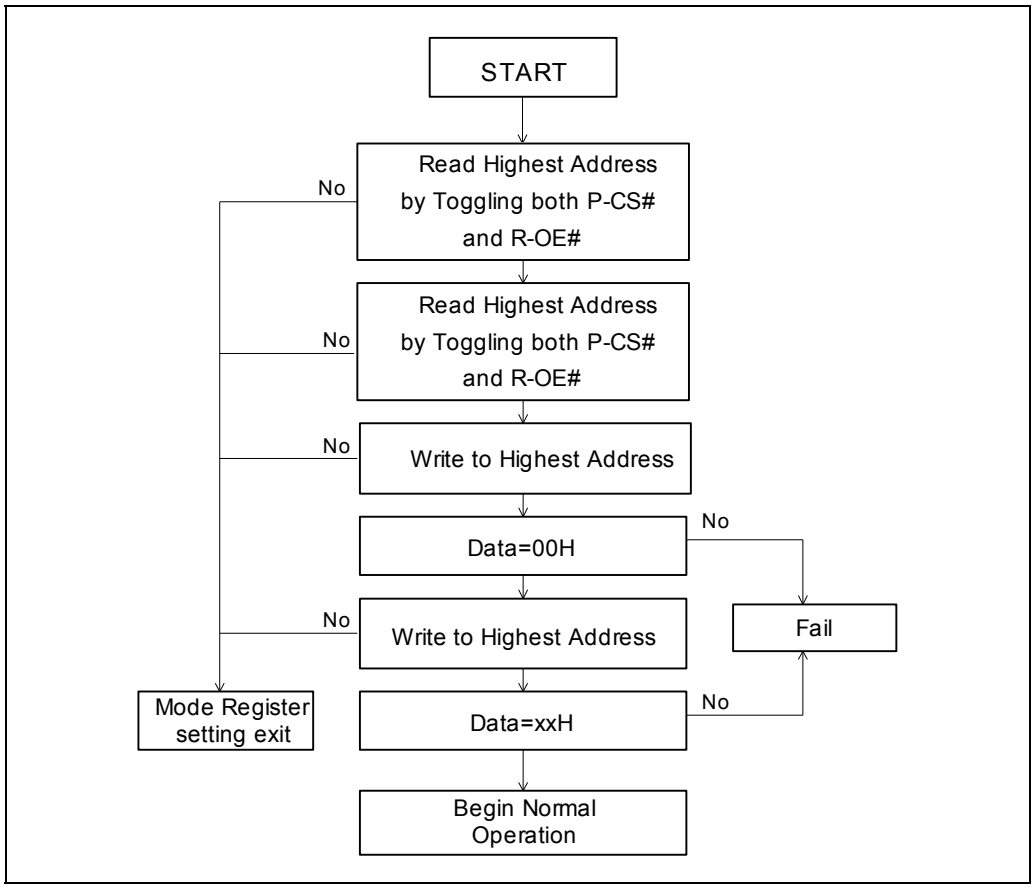


Figure 10. Mode Register Setting Flow Chart



NOTE: xxH=04H, 05H, 06H or 07H

12.2.2 Cautions for setting Mode Register

Since, for the Mode register setting, the internal counter status is judged by toggling P-CS# and R-OE#, toggle P-CS# at every cycle during entry (read cycle twice, write cycle twice), and toggle R-OE# like P-CS# at the first and second read cycles. If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the Mode register is not performed correctly.

When the highest address is read consecutively three or more times, the Mode register setting entries are not performed correctly. (Immediately after the highest address is read, the setting of the Mode register is not performed correctly.) Perform the setting of the Mode register after power application or after accessing other than the highest address.

Once the refresh density has been set in the Mode register, these settings are retained until they are set again, while applying the power supply. However, the Mode register setting will become undefined if the power is turned off, so set the Mode register again after power application.

12.3 Low Power mode

In addition to the regular Standby mode with a full density data hold, Low Power mode performs partial density data refresh or zero density data refresh.

The Low Power mode allows customers to turn off sections of the PSRAM die to save refresh current. The PSRAM die is divided into four sections allowing certain sections to be refreshed with P-Mode tied Low.

In regular Standby mode, both P-CS# and P-Mode are high level. But in Low Power mode, P-Mode is low level. In Low Power mode, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Low Power mode. Refer to Figure 8, “Timing Waveform for Power up sequence” on page 26 for timing charts. When the density has been to set to 16 Mbits, 8 Mbits, or 4 Mbits in Low Power mode, it is not necessary to perform initialization to return to normal operation from Low Power mode. For timing charts, refer to Figure 11, “Low Power mode -Entry/Exit (16/ 8/ 4/ 0 Mbits)”

Figure 11. Low Power mode -Entry/Exit (16/ 8/ 4/ 0 Mbits)

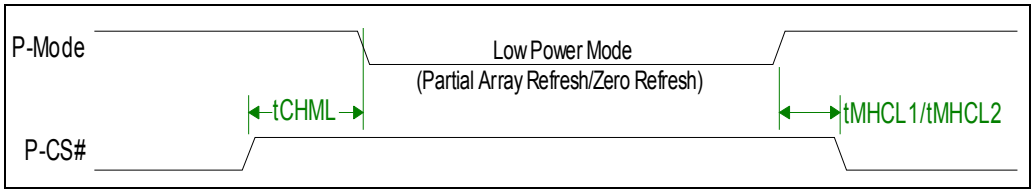


Table 16. Low Power mode-Entry/Exit

Parameter	Description	Min	Max	Unit
t_{CHML}	Low Power mode entry, P-CS# high level to P-Mode# Low level	0	-	ns
t_{MHCL1}	Low Power mode(16/8/4 Mbits hold) exit to normal operation, P-Mode High level to P-CS# Low level	30	-	ns
t_{MHCL2}	Low Power Mode(0 Mbit data hold) exit to normal operation, P-Mode High level to P-CS# Low level	200	-	us

NOTES:
1. t_{MHCL1} is the time it takes to return to normal operation from Low Power Mode (data hold: 16 /8 /4 Mbits).
2. t_{MHCL2} is the time it takes to return to normal operation from Low Power Mode (0 Mbits data hold).

Appendix A Write State Machine

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for the Write State Machine details.

Appendix B Common Flash Interface

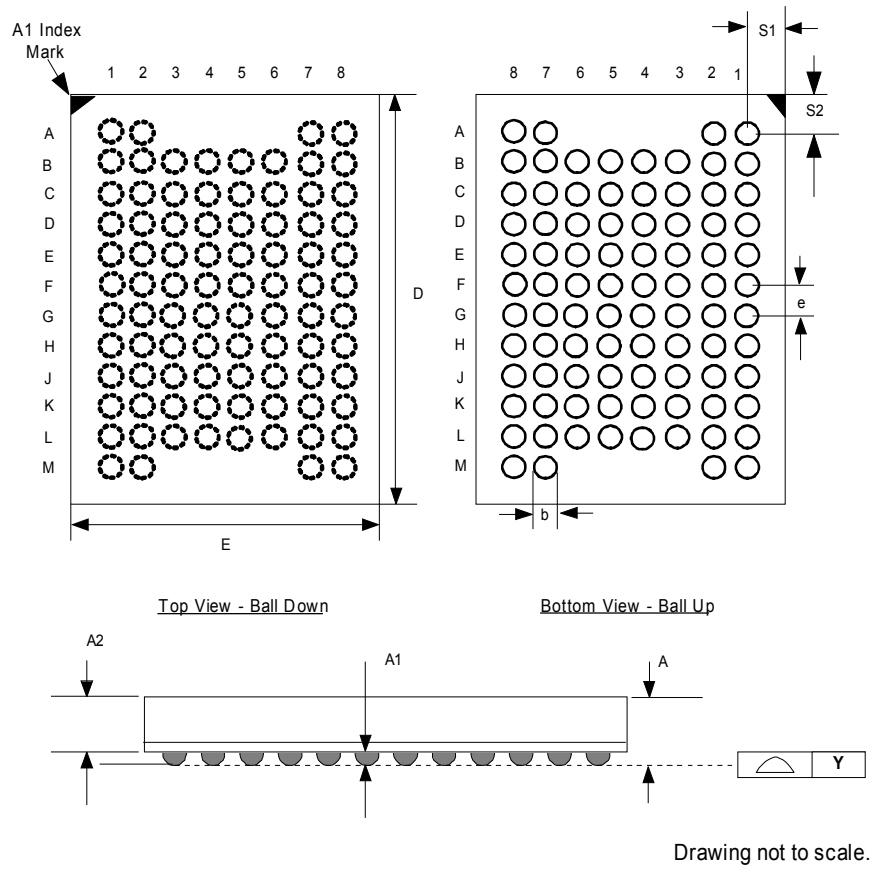
Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for the Common Flash Interface details.

Appendix C Flash Flowcharts

Refer to the *1.8 Volt Intel® Wireless Flash Memory Datasheet* (order number 290701) for the Flash Flowchart details.

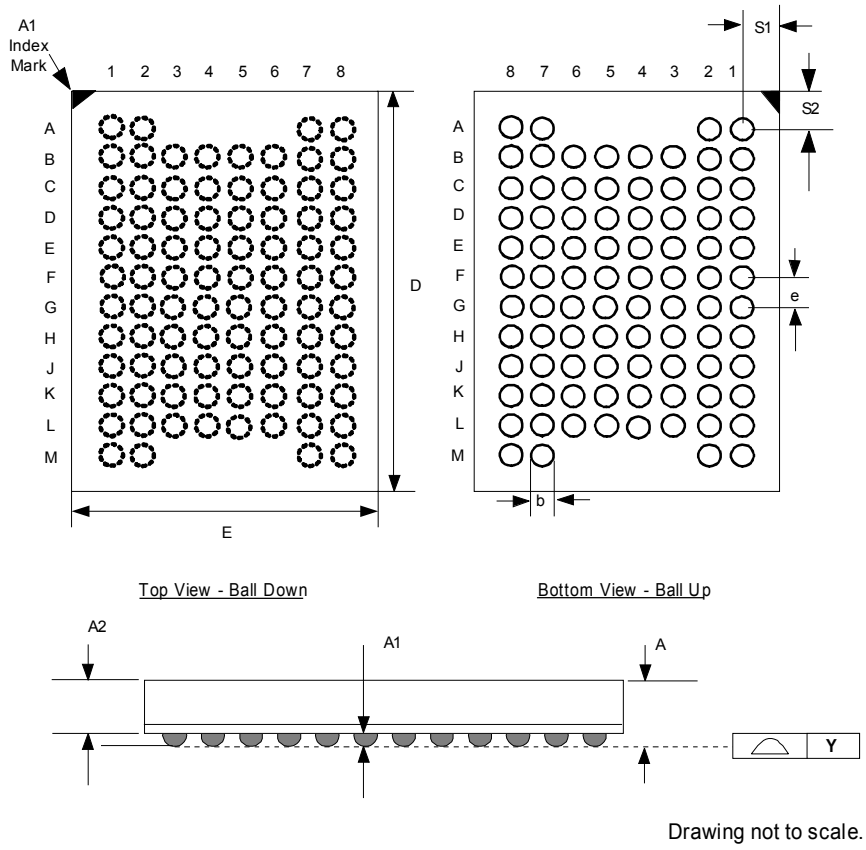
Appendix D Mechanical Package Information

Figure 12. 80-Active Ball Single or Double-Die Stacked-CSP Mechanical Specifications



		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

Figure 13. 80-Active Ball Triple-Die Stacked-CSP Mechanical Specifications



		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.400				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

Appendix E Additional Information

Order Number	Document
290701	*1.8 Volt Intel® Wireless Flash Memory (W18) Datasheet*
251407	*64-Mbit 1.8 Volt Intel® Wireless Flash Memory Stacked-CSP Family*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel flash memory products, software and tools, visit our website at http://developer.intel.com/design/flash.

Appendix F Ordering Information

F.1 128-Mbit W18 + 32-Mbit PSRAM Stacked-CSP Family Device Name Decoder

Figure 14 shows the decoder for products in this SCSP family with both flash and PSRAM. Figure 15 shows the decoder for products in this SCSP family with flash die only (no RAM).

Figure 14. Decoder for Flash+RAM SCSP Device Name

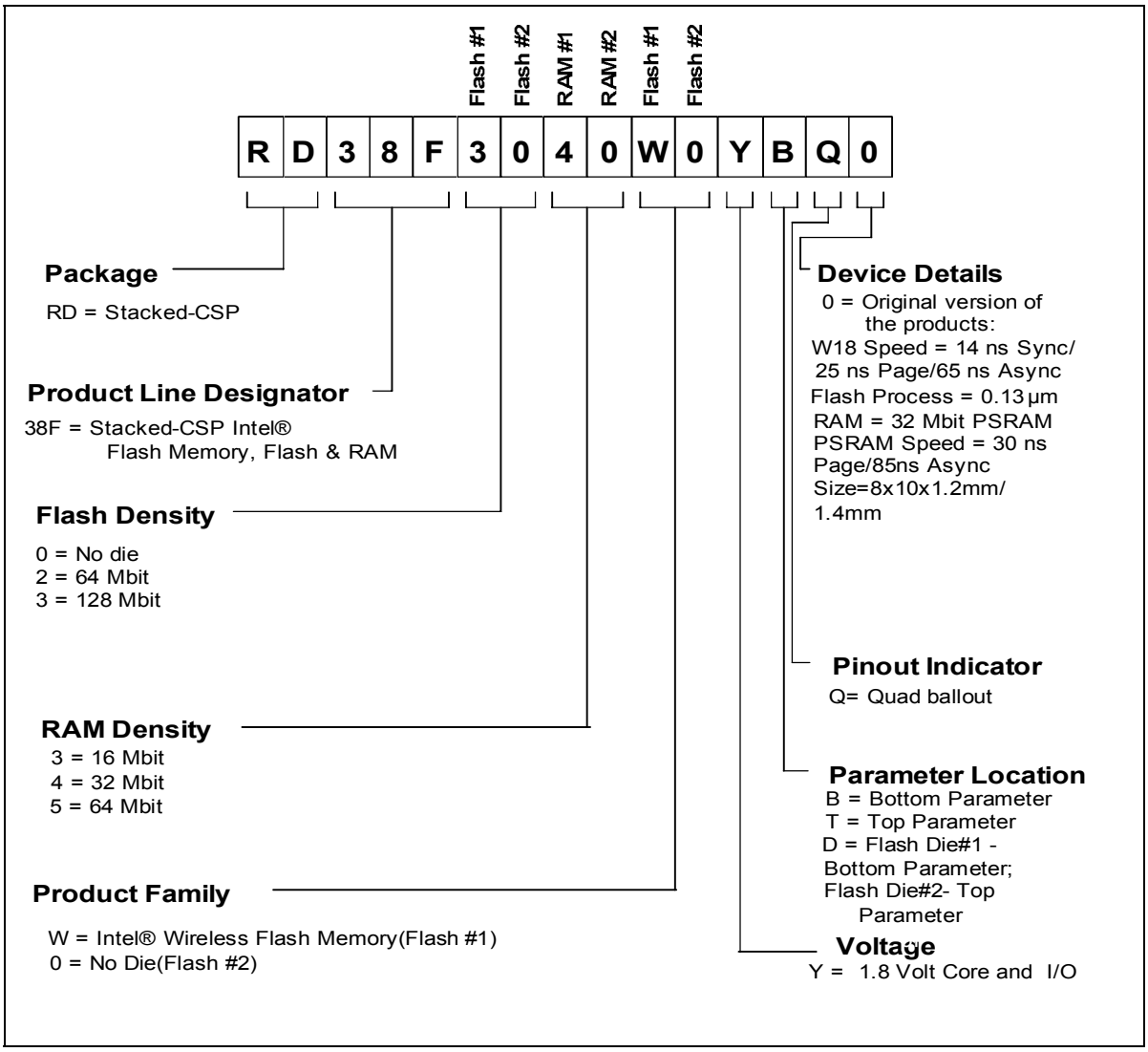
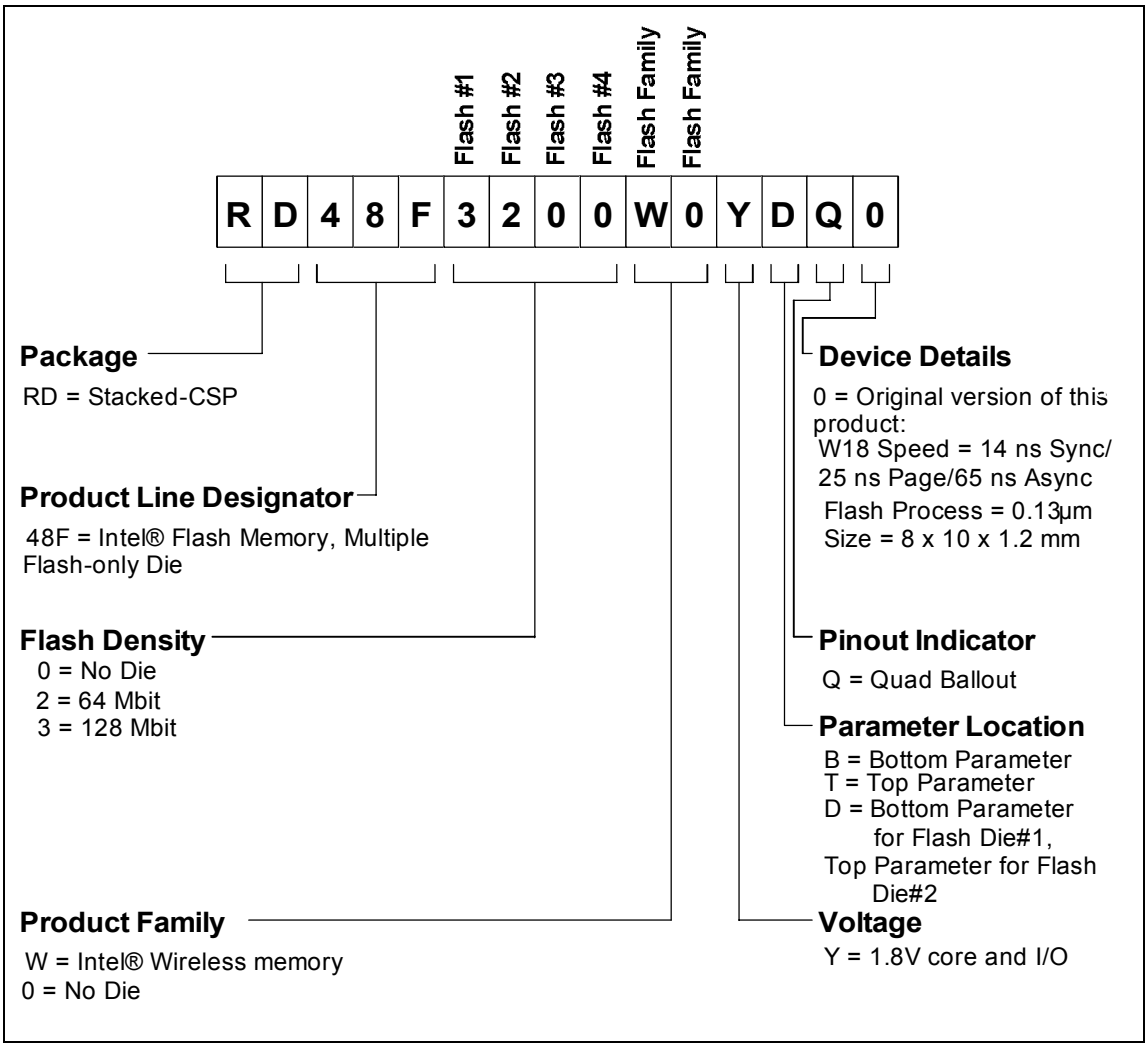


Figure 15. Decoder for Flash-Only SCSP Device Name



F.2 128-Mbit W18 + 32-Mbit PSRAM Stacked-CSP Family Device Name List

Table 17 shows the complete list of device names for products with single flash die in this SCSP family according to boot configuration.

Table 18 shows the complete list of device names for products with double flash die. Flash die#1 is configured bottom parameter while flash die#2 is configured top parameter. See Section 2.5, "Flash Memory Map and Partitioning" on page 13 for flash memory map and partitioning details of devices with double flash dies.

Table 17. Single Flash Die SCSP Device Name List

Product	Bottom Parameter Configuration Device Name	Top Parameter Configuration Device Name
128W18	RD48F3000W0YBQ0	RD48F3000W0YTQ0
128W18+32PSRAM	RD38F3040W0YBQ0	RD38F3040W0YTQ0

Table 18. Double Flash Die SCSP Device Name List

Product	Device Name
128W18B+64W18T	RD48F3200W0YDQ0
128W18B+64W18T+32PSRAM	RD38F3240WWYDQ0
128W18B+128W18T	RD48F3300W0YDQ0
128W18B+128W18T+32PSRAM	RD38F3340WWYDQ0