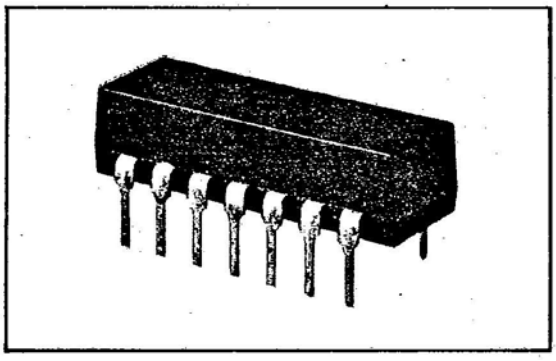
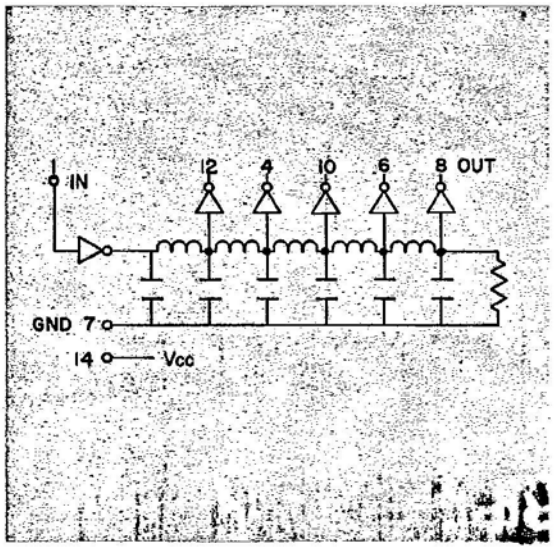
ACTIVE

AUTO INSERTABLE DIP DDM

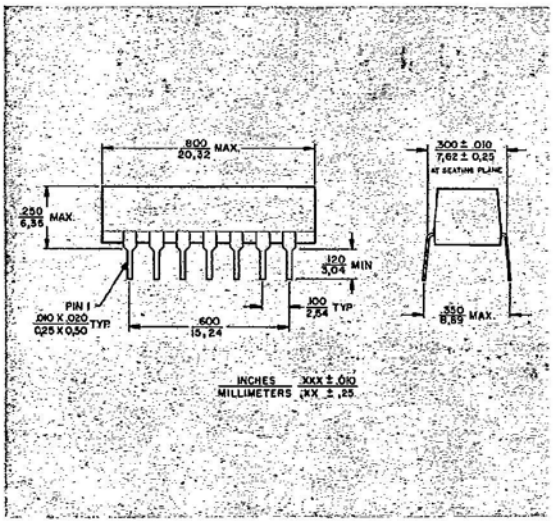


- AUTOMATICALLY INSERTABLE PACKAGE
- 14 PIN INDUSTRY STANDARD PINOUT
- 5 EQUALLY SPACED TAPS
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION



Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns max.)
24001	25.0	5.0	4.0
24002	30.0	6.0	4.0
24003	35.0	7.0	4.0
24004	40.0	8.0	4.0
24005	45.0	9.0	4.0
24006	50.0	10.0	4.0
24007	60.0	12.0	4.0
24008	75.0	15.0	4.0
24009	100.0	20.0	4.0
24010	125.0	25.0	4.0
24011	150.0	30.0	4.0
24012	200.0	40.0	4.0
24013	250.0	50.0	4.0

Delay Tolerance: ±2ns or ±5%, whichever is greater



Unused Pins not for external connection and may be removed upon request.

INPUT TEST CONDITIONS @25°C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 40% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

Refer to Pg. 12 for Waveform Definitions

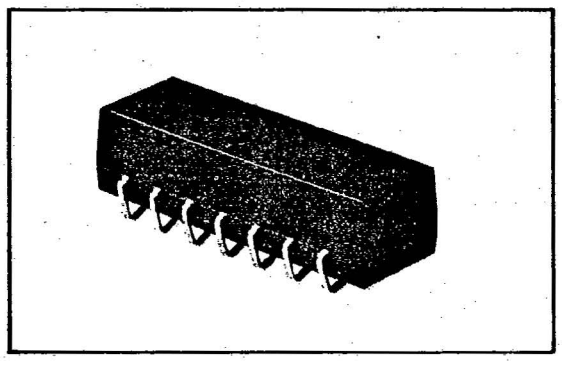
Pulse Engineering

P.O. BOX 12235, SAN DIEGO, CA 92112, (619) 268-2400

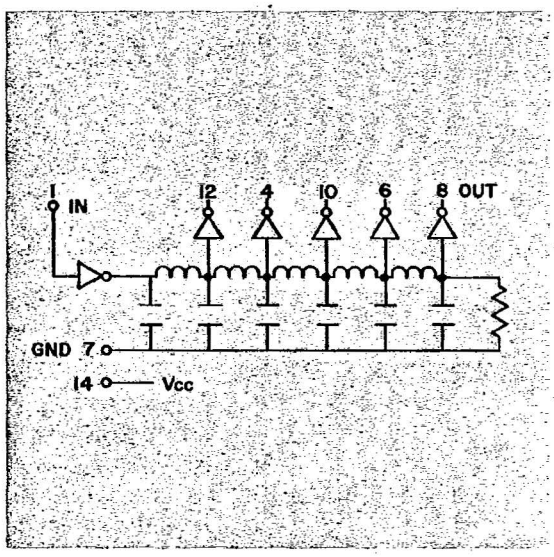
T-47-13

ACTIVE

SURFACE MOUNT DDM

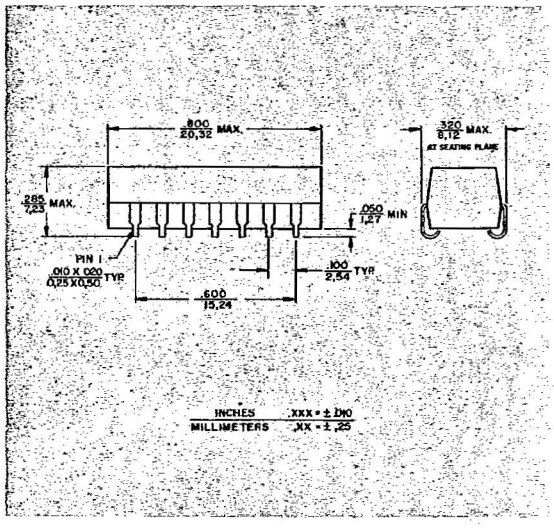


- SURFACE MOUNTABLE PACKAGE
- 14 PIN INDUSTRY STANDARD PINOUT
- 5 EQUALLY SPACED TAPS
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION



Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns max.)
24051	25.0	5.0	4.0
24052	30.0	6.0	4.0
24053	35.0	7.0	4.0
24054	40.0	8.0	4.0
24055	45.0	9.0	4.0
24056	50.0	10.0	4.0
24057	60.0	12.0	4.0
24058	75.0	15.0	4.0
24059	100.0	20.0	4.0
24060	125.0	25.0	4.0
24061	150.0	30.0	4.0
24062	200.0	40.0	4.0
24063	250.0	50.0	4.0

Delay Tolerance: ±2ns or ±5%, whichever is greater



Note: Gull-wing configuration available upon request.

INPUT TEST CONDITIONS @25°C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 40% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

Refer to Pg. 12 for Waveform Definitions

Pulse Engineering

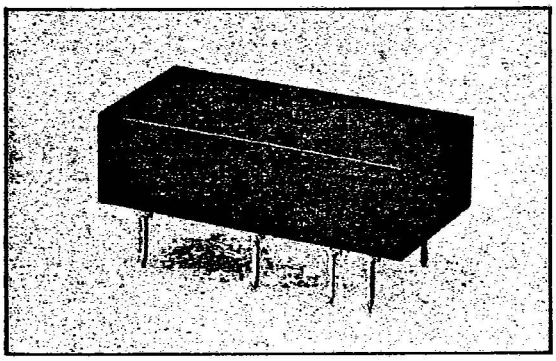
P.O. BOX 12235, SAN DIEGO, CA 92112, (619) 268-2400

PULSE ENGINEERING INC 69 DE 7428894 0000541 4

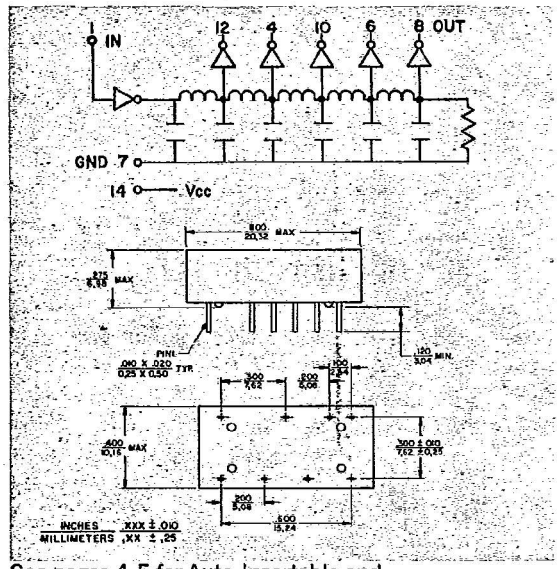
T-47-13

ACTIVE

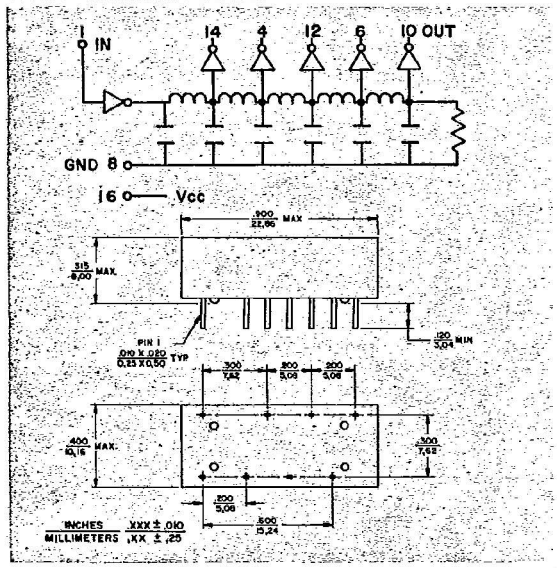
INDUSTRY STANDARD 5-TAP DDM



- 14 OR 16 PIN DIL PACKAGE
- INDUSTRY STANDARD PINOUTS
- 5 EQUALLY SPACED TAPS
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION



See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.



14 PIN

Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21197	25	5	3
21198	50	10	3
21741	60	12	3
21818	75	15	3
21199	100	20	3
21712	125	25	4
21212	150	30	4
21213	200	40	4
21214	250	50	4
21819	300	60	5
21820	400	80	5
21821	500	100	6

16 PIN

Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21215	25	5	3
21216	50	10	3
21217	100	20	3
21218	150	30	4
21219	200	40	4
21220	250	50	4

Delay Tolerance: ±2ns or ±5%, whichever is greater

INPUT TEST CONDITIONS @25°C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 40% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

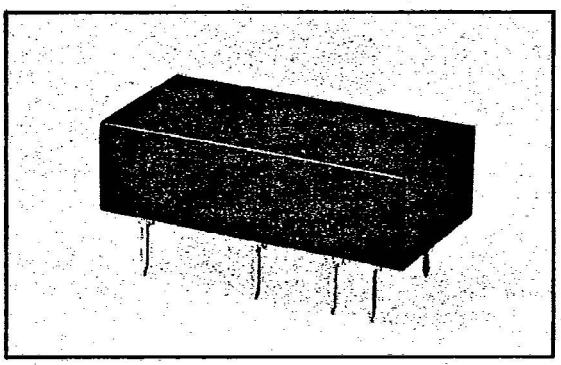
Refer to Pg. 12 for Waveform Definitions

Pulse Engineering

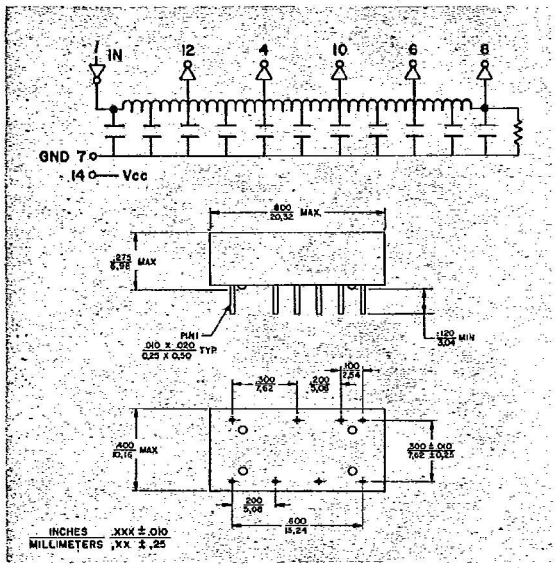
P.O. BOX 12235, SAN DIEGO, CA 92112, (619) 268-2400

ACTIVE

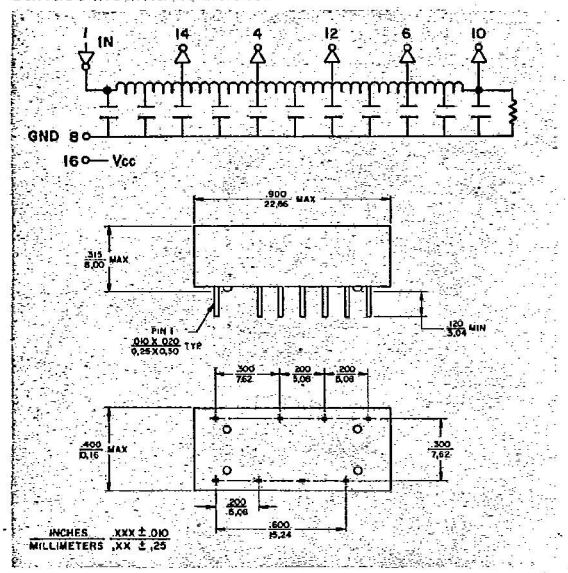
HIGH PERFORMANCE 5-TAP DDM



- LEADING AND TRAILING EDGE PRECISION
- TIGHTEST DELAY TOLERANCES
- 5 EQUALLY SPACED TAPS
- 14 OR 16 PIN DIL PACKAGE
- INDUSTRY STANDARD PINOUTS
- TTL/DTL COMPATIBLE



See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.



14 PIN

Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21468	25 ± 2.0	5 ± 1.5	3.0
21385	50 ± 2.0	10 ± 1.5	3.0
21386	100 ± 5.0	20 ± 2.0	3.0
21387	150 ± 6.0	30 ± 2.0	3.0
21388	200 ± 10.0	40 ± 2.0	4.0
21389	250 ± 12.5	50 ± 3.5	4.0
21347	500 ± 25.0	100 ± 5.0	5.0

16 PIN

Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21417	25 ± 2.0	5 ± 1.5	3.0
21418	50 ± 2.0	10 ± 1.5	3.0
21419	100 ± 5.0	20 ± 2.0	3.0
21420	150 ± 6.0	30 ± 2.0	3.0
21421	200 ± 10.0	40 ± 2.0	4.0
21422	250 ± 12.5	50 ± 3.5	4.0

INPUT TEST CONDITIONS @25°C

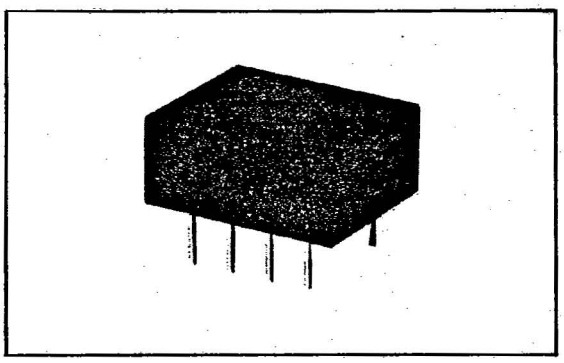
Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 20% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

Refer to Pg. 12 for Waveform Definitions

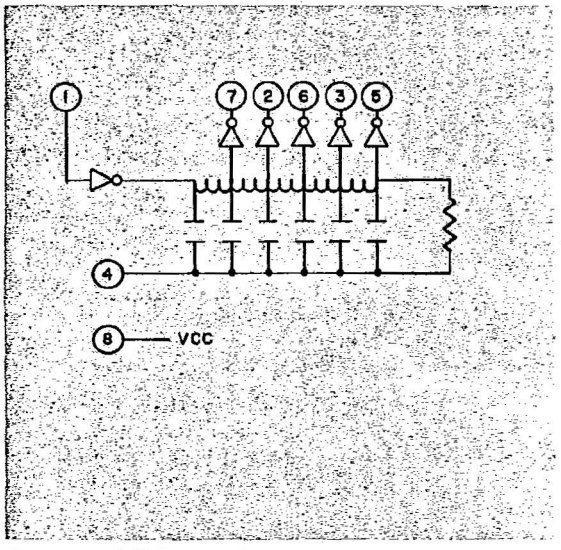
ACTIVE

T-47-13

MINI 5-TAP DDM



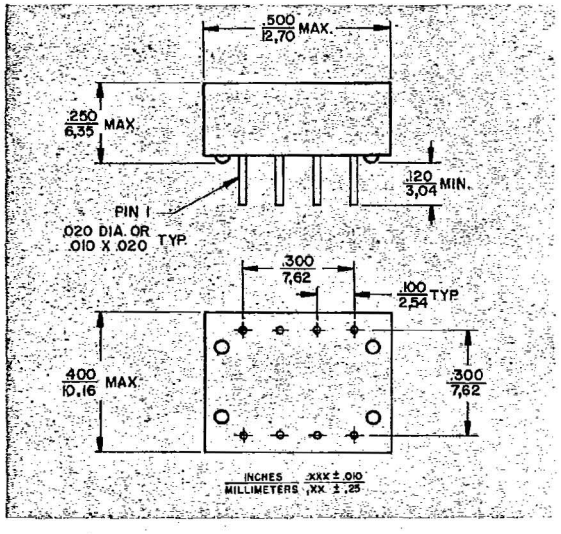
- SMALL SIZE—½" LONG 8 PIN PACKAGE
- 5 EQUALLY SPACED TAPS
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION
- INDUSTRY STANDARD PINOUT



See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.

Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns max.)
21901	25.0	5.0	4.0
21902	30.0	6.0	4.0
21903	35.0	7.0	4.0
21904	40.0	8.0	4.0
21905	45.0	9.0	4.0
21906	50.0	10.0	4.0
21907	60.0	12.0	4.0
21908	75.0	15.0	4.0
21909	100.0	20.0	4.0
21910	125.0	25.0	4.0
21911	150.0	30.0	4.0
21912	200.0	40.0	4.0
21913	250.0	50.0	4.0

Delay Tolerance: ±2ns or ±5%, whichever is greater



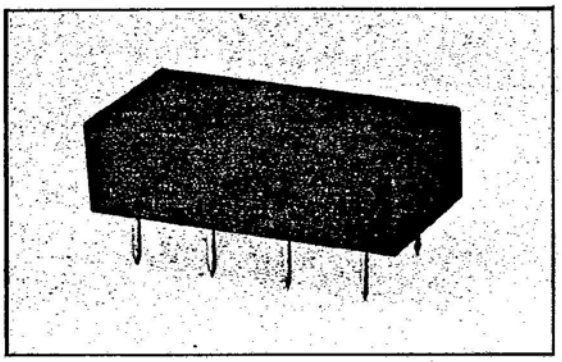
INPUT TEST CONDITIONS @25°C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 40% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

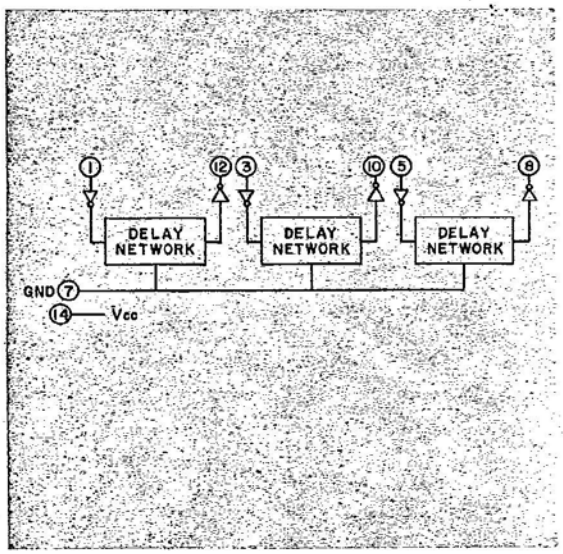
Refer to Pg. 12 For Waveform Definitions

ACTIVE

TRIPLE DDM



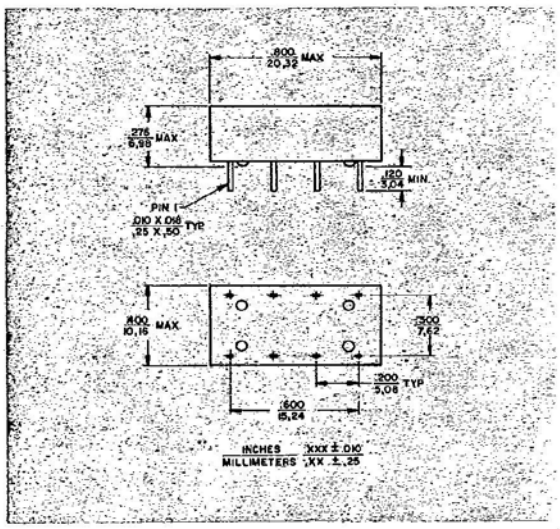
- 14 PIN DIL PACKAGE
- 3 INDEPENDENT EQUAL DELAYS
- NO TAPS
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION
- INDUSTRY STANDARD PINOUT



Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21260	5	N/A	3.0
21261	10	N/A	3.0
21262	20	N/A	3.0
21263	30	N/A	3.0
21264	40	N/A	3.0
21265	50	N/A	3.0
21266	60	N/A	4.0
21267	70	N/A	4.0
21268	80	N/A	4.0
21269	90	N/A	4.0
21270	100	N/A	4.0

Delay Tolerance: ±2ns or ±5%, whichever is greater

See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.



INPUT TEST CONDITIONS @25°C

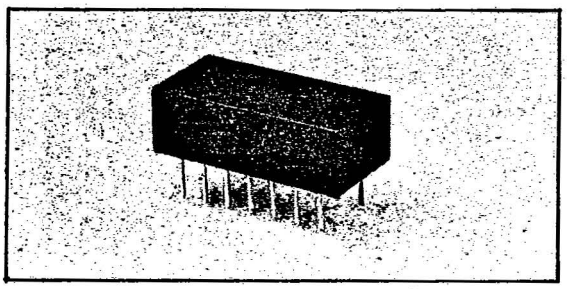
Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 100% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

Refer to Pg. 12 for Waveform Definitions

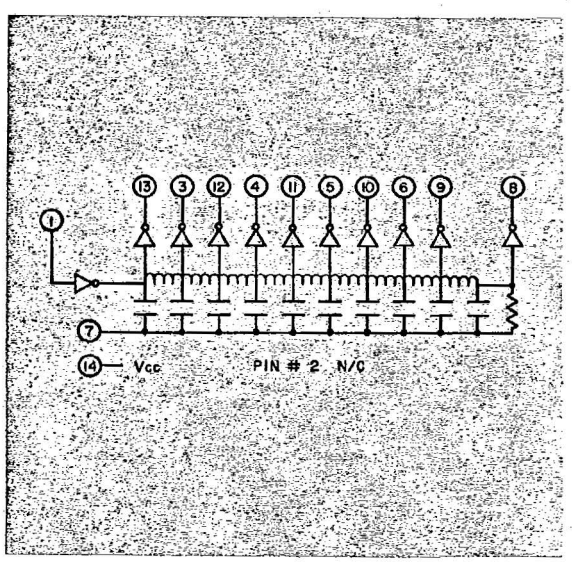
T-47-13

ACTIVE

INDUSTRY STANDARD 10-TAP 14-PIN DDM



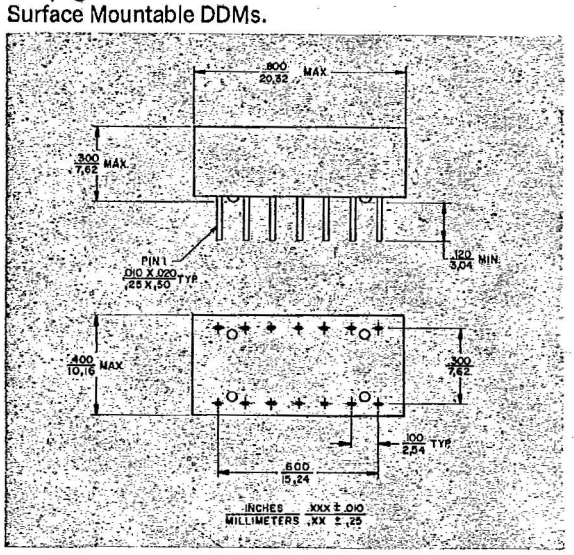
- 10 EQUALLY SPACED TAPS
- 14 PIN SPACE SAVING DIL PACKAGE
- INDUSTRY STANDARD PINOUT
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION



Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns max.)
21781	50 NS	5.0 NS	4.0
21782	75 NS	7.5 NS	4.0
21783	100 NS	10.0 NS	4.0
21784	125 NS	12.5 NS	4.0
21785	150 NS	15.0 NS	4.0
21786	200 NS	20.0 NS	4.0
21787	250 NS	25.0 NS	4.0
21788	300 NS	30.0 NS	4.0
21789	350 NS	35.0 NS	4.0
21790	400 NS	40.0 NS	4.0
21791	500 NS	50.0 NS	4.0

Delay Tolerance: ±2ns or ±5%, whichever is greater

See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.



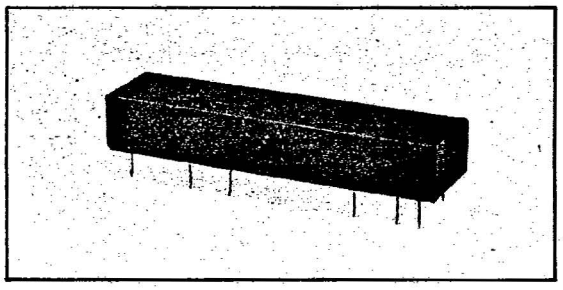
INPUT TEST CONDITIONS @25° C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 30% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

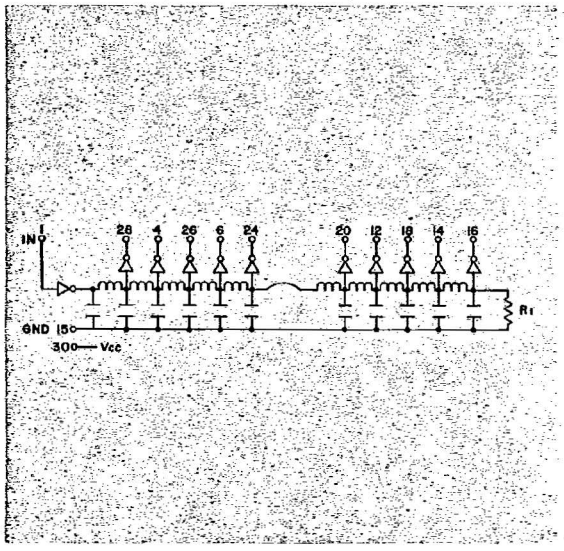
Refer to Pg. 12 for Waveform Definitions

ACTIVE

INDUSTRY STANDARD 10-TAP 30-PIN DDM



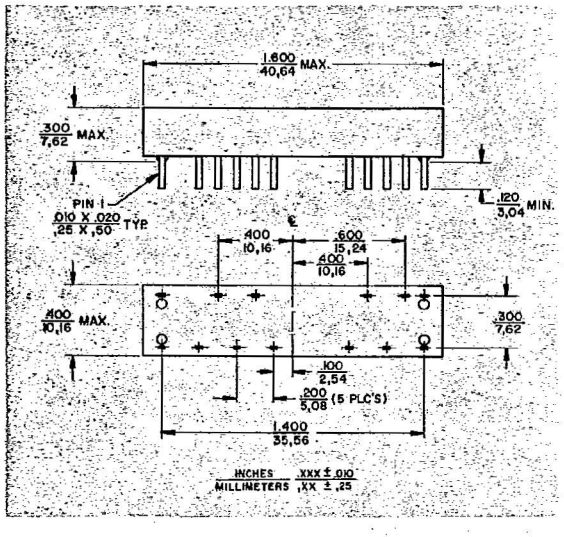
- 10 EQUALLY SPACED TAPS
- 30 PIN DIL PACKAGE
- INDUSTRY STANDARD PINOUT
- TTL/DTL COMPATIBLE
- LEADING EDGE PRECISION



Part Number	Total Delay (ns)	Tap Delay (ns)	Rise Time (ns Max)
21310	50	5	4
21311	100	10	4
21312	150	15	4
21313	200	20	4
21314	250	25	4
21315	300	30	5
21316	400	40	6
21317	500	50	6

Delay Tolerance: ±2ns or ±5%, whichever is greater

See pages 4-5 for Auto-Insertable and Surface Mountable DDMs.



INPUT TEST CONDITIONS @25°C

Pulse Voltage	3.0V
Rise Time	3.0ns
Pulse Width	Min 30% of Td
PRR	3 x twi Min.
Vcc	5.0V D.C.

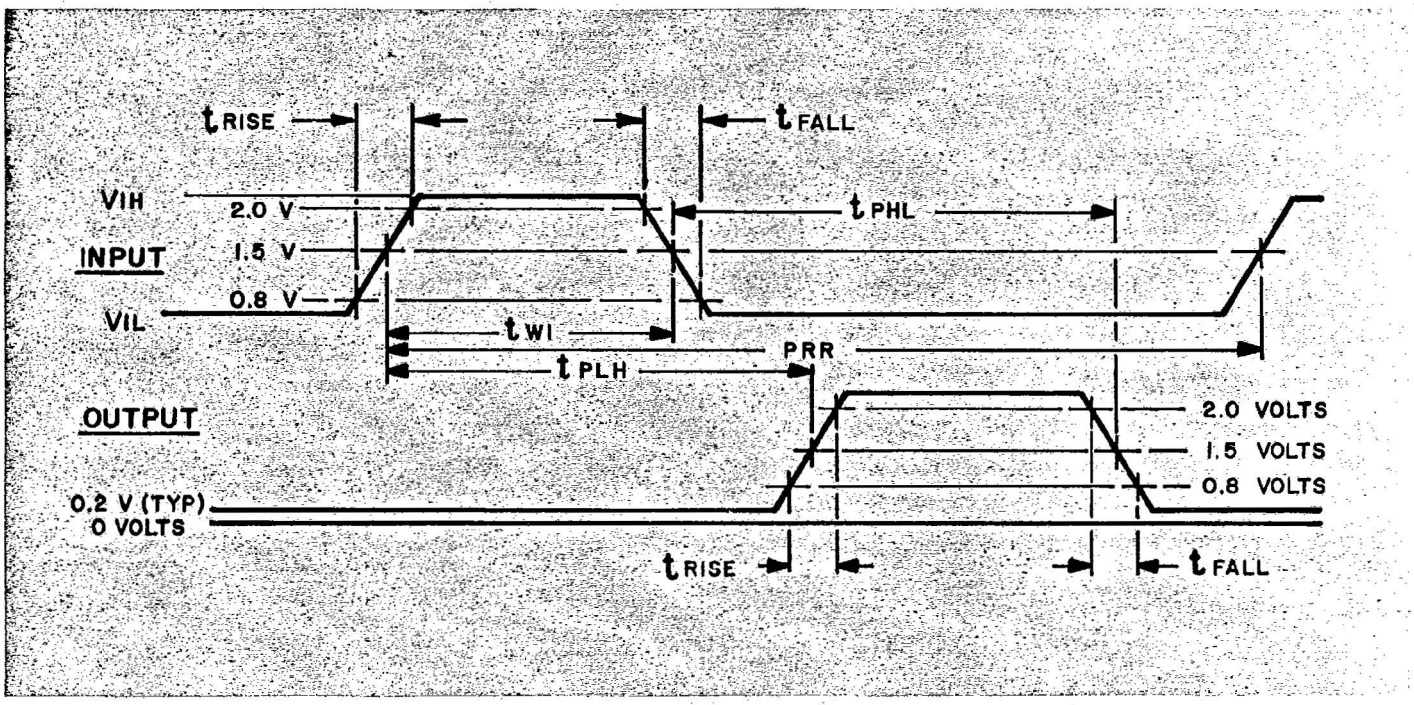
Refer to Pg. 12 for Waveform Definitions

Pulse Engineering

P.O. BOX 12235, SAN DIEGO, CA 92112, (619) 268-2400

T-47-13

ACTIVE DELAY LINES—TEST CONDITIONS



ACTIVE DEFINITIONS

V_{IH} HIGH INPUT VOLTAGE—normal condition is 5.5V Max.

V_{IL} LOW INPUT VOLTAGE—normal condition is ground.

t_{PLH} DELAY TIME measured at the 1.5V level of the "low to high" edge between input and output pulses.

t_{PHL} DELAY TIME measured at the 1.5V level of the "high to low" edge between input and output pulses.

t_{RISE} PULSE RISE TIME measured from 0.8V to 2.0V on the rising edge of the pulse

t_{FALL} PULSE FALL TIME measured from 2.0V to 0.8V on the falling edge of the pulse

t_{WI} INPUT PULSE WIDTH measured at the 1.5V level on input pulse

PRR PULSE REPETITION RATE measured at the 1.5V level from input pulse to next occurring input pulse

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Condition	Min.	Nom.	Max.	Units
V_{CC}	Supply Voltage				+7.0	Volts
V_{IH}	High Level Input Voltage				+5.5	Volts
T_A	Operating Temperature Range	Free Air	0	+25	+70	°C
	Storage Temperature Range	Free Air	−55		+125	°C
N_H	Normalized Fan-out (per Tap)	V_{CC} = Max., Logic 1			20	Loads
N_L	Normalized Fan-out (per Tap)	V_{CC} = Max., Logic 0			10	Loads