



## A Complete 2.5 Gbits/s Fiber-Optic Receiver for SONET Applications

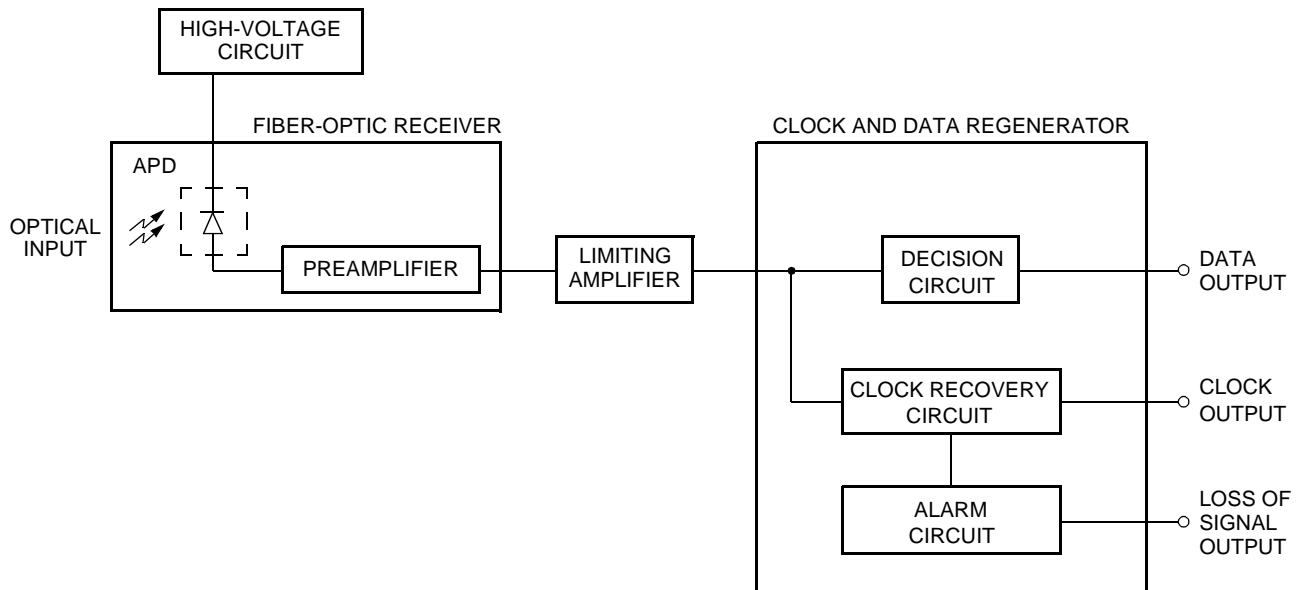
### Introduction

This technical note describes a complete 2.5 Gbits/s fiber-optic receiver that will meet SONET requirements for OC-48 system applications. The complete receiver includes clock recovery and data regeneration. It has been designed around Lucent Technologies Microelectronics Group Optoelectronics unit 1319-Type High-Speed Fiber-Optic Receiver and the Transmission IC unit GaAs ICs.

A simplified circuit block diagram is shown in Figure 1. An InGaAs avalanche photodiode (APD) converts an incoming optical signal to an electrical current. The high-voltage circuit provides the proper high-voltage bias for the APD. The preamplifier stage is a transimpedance amplifier that amplifies the weak electrical current from the APD and converts it to a voltage output. The limiting amplifier

stage further amplifies the signal but also limits its output amplitude in order to remain within the maximum input limits of the next stage. The decision circuit decodes the incoming electrical signal into a digital logic output of ones and zeros, which represent the originally transmitted data. The clock-recovery circuit extracts a timing signal that is synchronized to the data rate. Finally, the alarm circuit detects a loss of signal condition and provides a logic-level output whenever the clock-recovery circuit is unable to recover a valid timing signal from the recovered electrical signal.

Figure 2 shows a complete 2.5 Gbits/s SONET/SDH optical receiver design. A fully assembled evaluation board is available from the Lucent Technologies Microelectronics Group Transmission IC unit. Please visit their Internet site at <http://www.lucent.com/micro/tic> for more details and contact information.



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Figure 1. System Block Diagram

Introduction (continued)

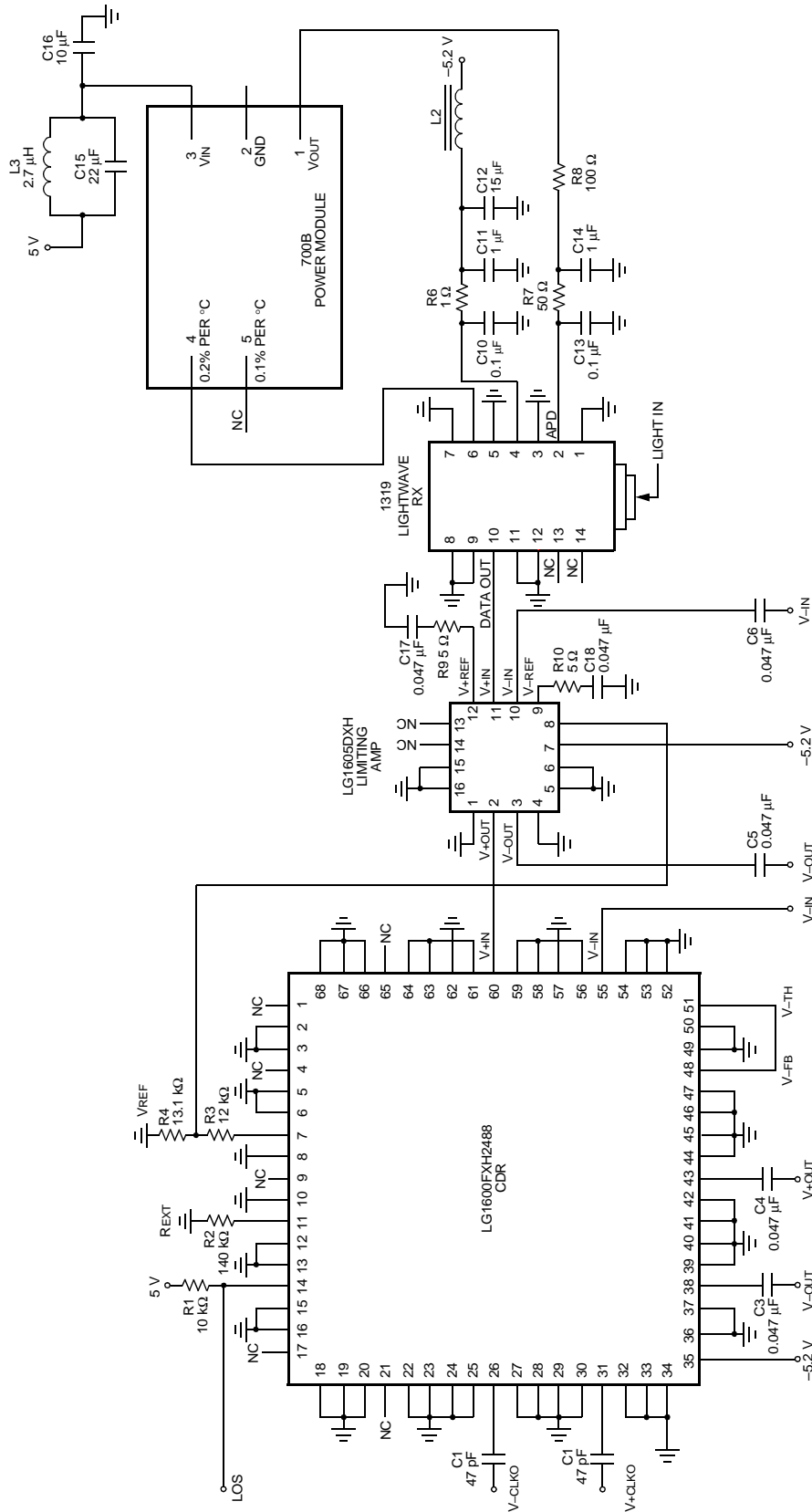


Figure 2. A Complete Lucent 2.5 Gbits/s SONET/SDH Receiver

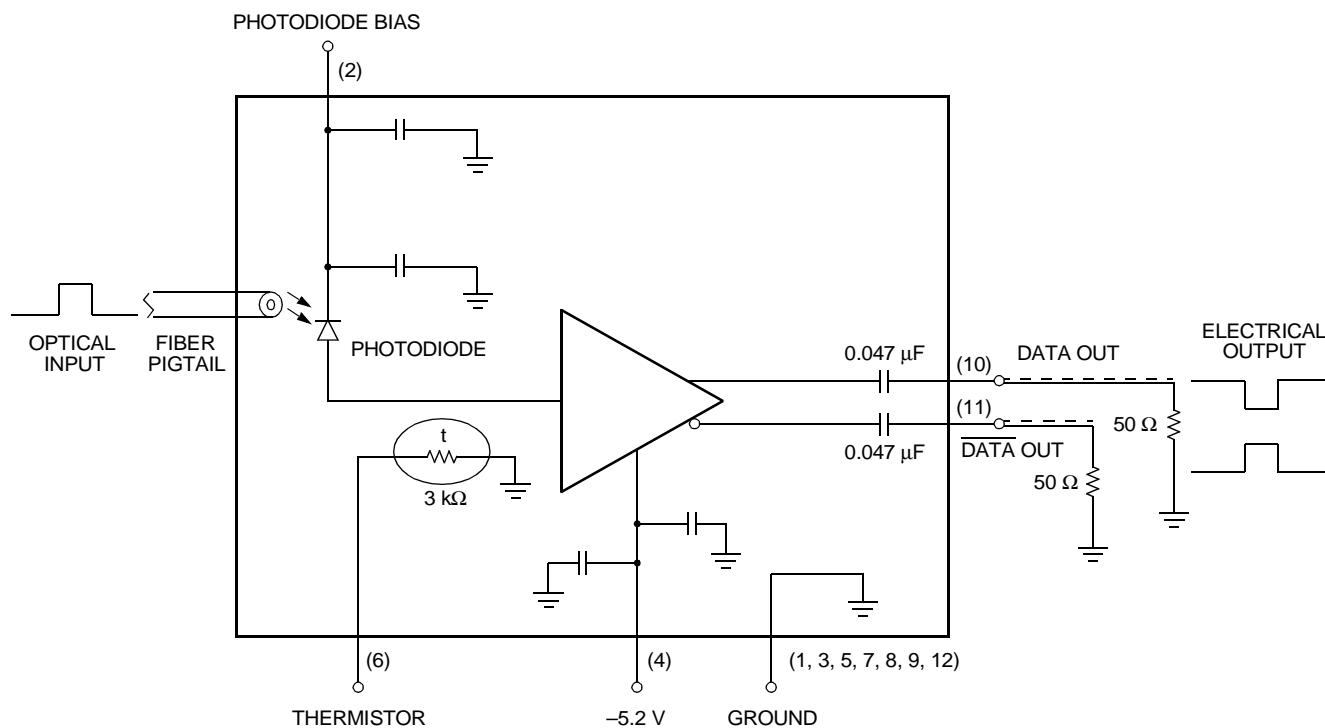
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## Fiber-Optic Receiver

The optical receiver function is provided by a Lucent 1319-Type Receiver. This unit consists of the APD photodetector and transimpedance amplifier contained within a metal and ceramic, 14-pin pigtailed package. It operates with optical input signals in the wavelength range of 1250 nm to 1600 nm. A simplified schematic of the receiver is shown in Figure 3. The receiver requires a  $-5\text{ V}$  power supply to provide electrical bias to the preamplifier IC as well as a positive, high-voltage, low-current power supply capable of providing up to approximately  $60\text{ V}$  of bias for the APD. For operation at temperatures other than  $25\text{ }^\circ\text{C}$ , the APD bias supply should provide a temperature-compensated output that matches the APD gain coefficient of  $0.18\%/^\circ\text{C}$ . A  $3\text{ k}\Omega$  resistance thermistor contained within the receiver package provides a means of monitoring the receiver temperature. Internal power supply filtering is

provided to minimize noise susceptibility. However, external filtering is highly recommended. The output of the receiver is ac-coupled through a  $0.047\text{ }\mu\text{F}$  capacitor. This output is designed to drive a  $50\text{ }\Omega$  impedance load.

The 1319 receiver is designed for operation at a data rate of  $2.5\text{ Gbits/s}$  and has a typical  $3\text{ dB}$  bandwidth of  $1.6\text{ GHz}$ . The minimum data rate for the receiver is approximately  $400\text{ MHz}$ . Its typical sensitivity at a data rate of  $2.5\text{ Gbits/s}$ , with an APD gain of 12, is  $-34\text{ dBm}$  at a bit error rate (BER) of  $3 \times 10^{-11}$ . The transimpedance of this receiver is  $1.25\text{ k}\Omega$  when operated at an APD gain of 12. At an optical input power of  $-30\text{ dBm}$  and an APD gain of 12, the APD generates an average photocurrent of approximately  $10\text{ }\mu\text{A}$ , resulting in an output voltage from the receiver of  $25\text{ mV}$  peak-to-peak.



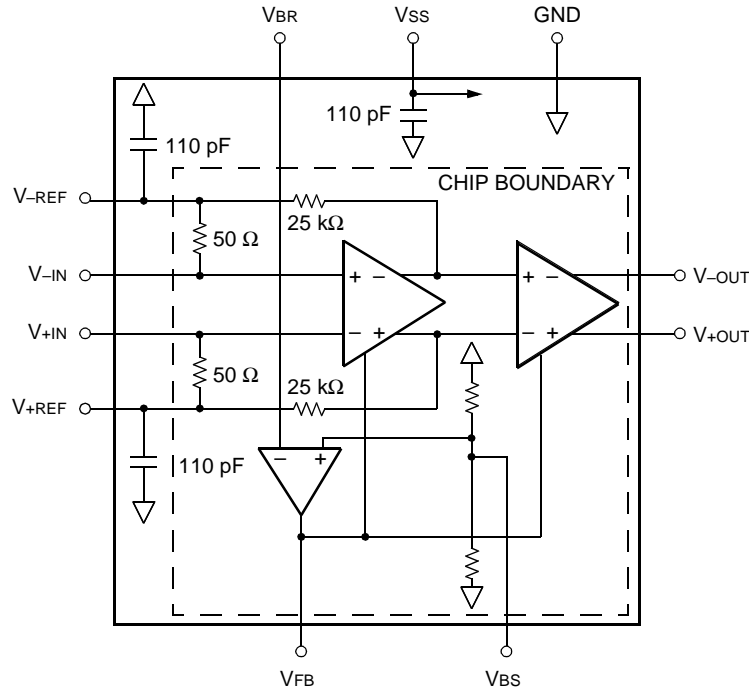
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Figure 3. 1319-Type High-Speed Fiber-Optic Receiver Schematic

**Limiting Amplifier**

The limiting amplifier is a Lucent part number LG1605DXB. The device is a wideband amplifier with differential inputs and outputs, manufactured using gallium arsenide (GaAs) technology. It has a 3 GHz bandwidth and provides a typical gain of 28 dB in a 50 Ω environment. It is supplied in a hermetically sealed, 16-lead, glass-metal surface-mount package.

Figure 4 shows a simplified schematic for this circuit. The differential inputs are terminated internally in 50 Ω to simplify connection to the signal source, and the outputs are designed to efficiently drive a 50 Ω load impedance.



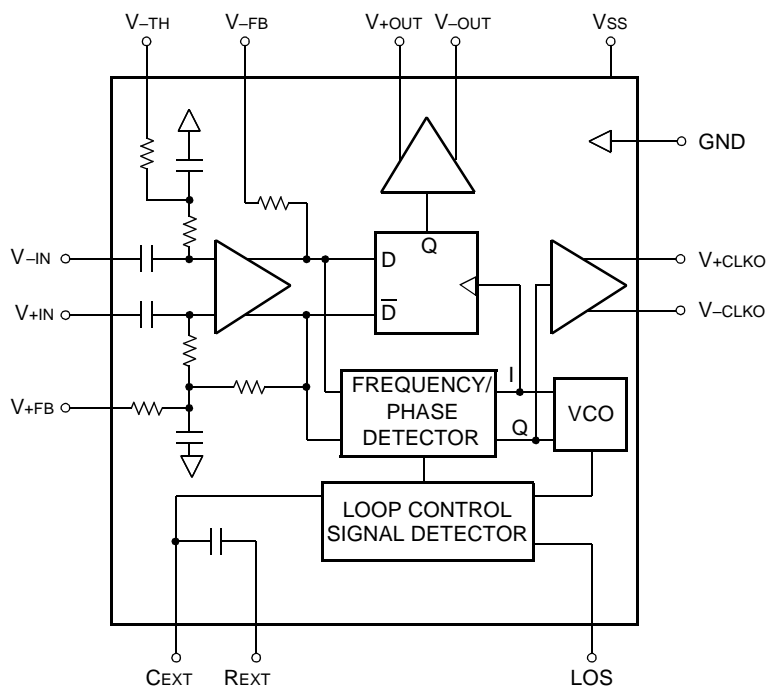
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**Figure 4. LG1605DXB Limiting Amplifier**

## Clock and Data Regenerator

The data-decision circuit, clock-recovery circuit, and loss of signal alarm function are provided by a single, 68-lead, hermetic, surface-mount package. The LG1600FXH is designed to regenerate a clean clock and data signal from a data input corrupted by jitter and intersymbol interference. This device utilizes phase-locked loop (PLL) technology to recover the clock signal from the input data signal. The PLL circuit is tuned at the factory for a 2.488 Gbits/s data rate (other data

rates are available), and output jitter performance exceeds SONET and ITU-T jitter tolerance requirements for OC-48/STM-16 systems. This device accepts single-ended or differential data inputs and are ac-coupled internally. The regenerated clock and data signals are available from complementary outputs that can be ac-coupled to provide a 50 Ω output match, or dc-coupled with 50 Ω to ground as required by the system application. Figure 5 shows a functional block diagram of the LG1600FXH clock and data regenerator IC.



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Figure 5. LG1600FXH Clock and Data Regenerator

## High-Voltage Power Supply\*

To establish the APD gain, the APD requires a high-voltage bias in the range of 50 V to 60 V, as mentioned previously. Additionally, the power supply output should be temperature-compensated to match the gain vs. temperature coefficient of the APD.

The Lucent 700B power module available from Lucent's Power Systems unit satisfies these criteria. This device is a dc-dc converter that operates from a +5 V supply and provides an adjustable dc output of 24 V to 97 V. The output voltage is adjusted by setting an on-board DIP switch. Selectable thermistor inputs allow output temperature compensation of either 0.1% or 0.2% per °C.

## Performance Issues

Although the circuit schematic for the complete receiver is straightforward, obtaining maximum performance requires careful attention to the details of the circuit layout and the operation of the fiber-optic receiver. This is especially true at 2.5 Gbits/s.

## Printed-Wiring Board

At 2.5 Gbits/s, the printed-wiring board (PWB) must be considered a critical part of the overall design. It is not necessary to use microwave materials for the PWB; however, a high-quality material with a well-controlled dielectric constant should be used.

To begin with, the mix of analog and digital functions, two different power supplies, and ground necessitates a multilayer circuit-board design. An extensive ground plane must be used throughout in order to provide the shortest current return paths as well as provide a means to establish controlled-impedance traces for the data signals (stripline or microstrip construction).

The differential data lines connecting the limiting amplifier to the clock and data regenerator must be straight, parallel, and equal in length. The single data line connecting the 1319 to the limiting amplifier should be as straight as possible. If this line must turn, a curved trace or an angled trace should be used. Do not make sharp 90-degree turns in the data lines.

\* See also AP98-080LWP, *Low-Cost, High-Voltage APD Bias Circuit with Temperature Compensation Application Note*.

All three major components are surface-mount type devices; therefore, surface-mount discrete components should be used as well. Power-supply filtering components should be placed as close as possible to the relevant device power-supply lead. If the complete receiver is built as a stand-alone element, then additional power-supply filtering should be used at a point where the power supplies are brought onto the receiver PWB. Also, the clock and data lines should be connected to the next circuit element via high-quality, RF connectors and coaxial cables.

## 1319 Receiver

APD receivers provide approximately 5 dB more sensitivity than PIN receivers. This differential does not occur without some additional complexity and cost. The additional sensitivity comes about because the APD is capable of providing internal gain, whereas the PIN operates at a gain of slightly less than one. But, to obtain the internal gain from an APD requires operating it with a rather large bias voltage—typically 50 V to 60 V for an InGaAs APD, while the PIN can often be operated from a rather low bias of 2 V to 3 V supplied internally by the receiver IC.

The gain function of the APD is also temperature-sensitive when it is operated with a fixed bias voltage. As the temperature of the APD changes, the gain will vary—typically 0.18%/°C change in temperature for the 1319 APD. When operating in the presence of a moderate optical input signal, this effect is relatively inconsequential. However, when operating near the receiver sensitivity limit, a change in temperature could cause the receiver bit-error rate to degrade to unacceptable levels. Therefore, it is necessary that the APD high-voltage bias supply has a means to automatically adjust the output voltage in response to temperature changes in the receiver. For this purpose, the 1319 receiver has an internal thermistor that can be used to monitor the receiver temperature. The thermistor has a nominal resistance of 3000  $\Omega$  at 25 °C. Table 1 shows the nominal thermistor resistance vs. temperature. If this thermistor is coupled to a power supply such as the Lucent 700B, which has a temperature-compensated output, then a temperature-independent gain can be established for the APD. Figure 6 shows a typical plot of the bias voltage required to maintain constant gain over the operating temperature range of 0 °C to 65 °C, the recommended case-operating temperature range of the 1319 receiver.

Performance Issues (continued)

Table 1. 1319-Type Receiver Thermistor Resistance vs. Temperature

T (°C)	R (Ω)	T (°C)	R (Ω)	T (°C)	R (Ω)	T (°C)	R (Ω)
0	9796	20	3748	40	1598	60	746.3
1	9310	21	3583	41	1535	61	719.9
2	8851	22	3426	42	1475	62	694.7
3	8417	23	3277	43	1418	63	670.4
4	8006	24	3155	44	1363	64	647.1
5	7618	25	3000	45	1310	65	624.7
6	7252	26	2872	46	1260	66	603.3
7	6905	27	2570	47	1212	67	582.6
8	6576	28	2633	48	1167	68	562.8
9	6285	29	2523	49	1123	69	543.7
10	5971	30	2417	50	1081	70	525.5
11	5692	31	2317	51	1040	71	507.8
12	5427	32	2221	52	1002	72	490.9
13	5177	33	2130	53	965	73	474.7
14	4939	34	2042	54	929.6	74	459
15	4714	35	1969	55	895.8	75	444
16	4500	36	1880	56	863.3	76	429.5
17	4297	37	1805	57	832.2	77	415.6
18	4105	38	1733	58	802.3	78	402.2
19	3922	39	1664	59	773.7	79	389.3

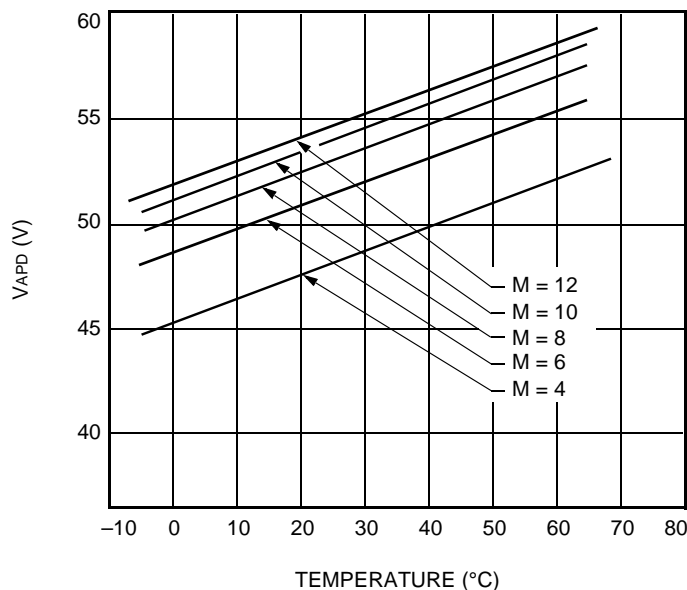


Figure 6. Gain vs. APD Bias as a Function of Temperature for a Typical 1319-Type Receiver

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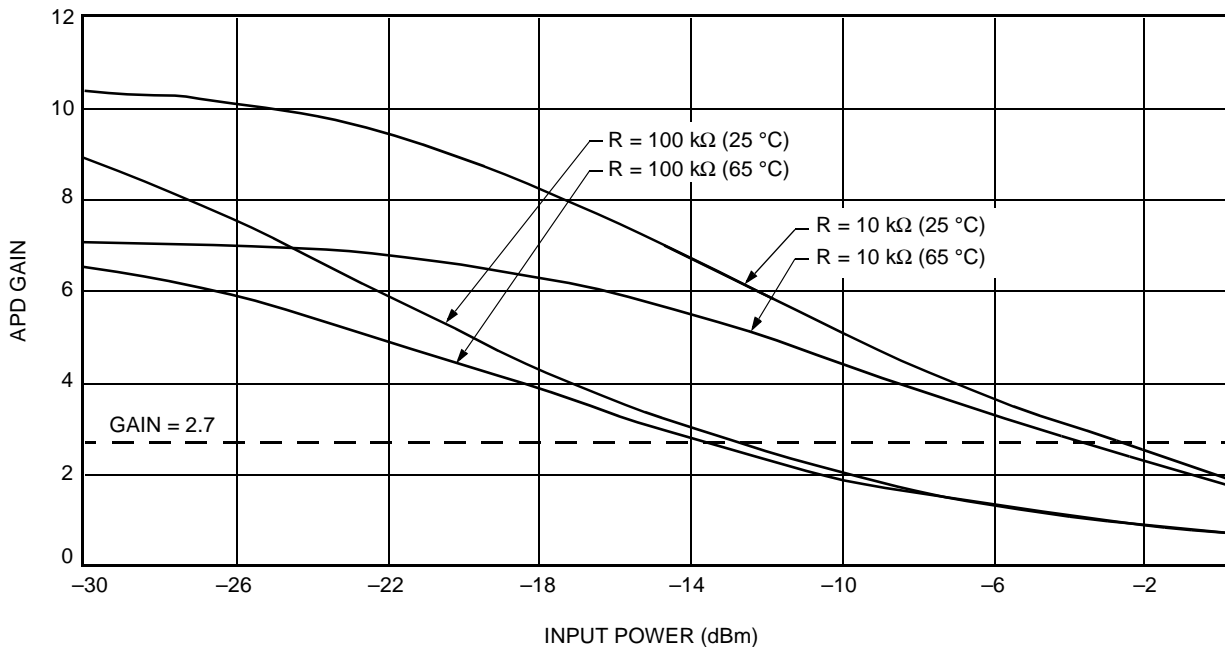
**Performance Issues** (continued)

It is common practice to place a resistor in series between the high-voltage supply and the APD bias pin on the receiver. The resistor provides some protective isolation for the receiver as well as output short-circuit protection for the power supply. This series resistor can also be used to monitor the optical input power for alarm or surveillance applications by measuring the voltage drop across the resistor, which results from photocurrent flow through the resistor. The value for this resistor needs to be chosen in terms of how the receiver will ultimately be used, particularly when high optical input powers are involved. If the series resistance value is too great, the voltage drop across the resistor due to photocurrent flow can reduce the APD bias voltage and, ultimately, the APD gain. If this gain reduction is too large, the performance of the receiver can be affected to the point where significant bit errors are introduced (Figure 7 shows this effect). Here, APD gain is plotted versus optical input power for a 10 kΩ and a 100 kΩ resistor at both 25 °C and 65 °C. The dashed line at gain = 2.7 is the minimum gain at which

the APD is capable of operating. It can be seen that with the 10 kΩ resistor, very little gain compression occurs. However, with the 100 kΩ resistor, the APD gain actually drops below the gain 2.7 cutoff point, around -13 dBm. This means that with a 100 kΩ series resistor, optical input powers higher than -13 dBm would actually cause the receiver to fail.

This plot also shows that with a 10 kΩ series resistor, there is a beneficial gain compression at the higher optical input powers. The initial gain of approximately 10 at low optical input powers has dropped to approximately 4 at -10 dBm. This prevents overload of the 1319 receiver as well as overload of the subsequent amplifier stage following the 1319 receiver.

In optically amplified systems, the optical input signal to the receiver can easily exceed 0 dBm and in some instances even exceed 3 dBm. In these applications, it is recommended that the series resistor value be reduced to approximately 5 kΩ to prevent excessive gain compression.



**Figure 7. APD Gain vs. Input Power**

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## Receiver Performance

This basic receiver system has been built and tested by several Lucent customers. Figure 8 is a BER plot at 2.4 Gbits/s versus optical input power for this receiver system measured at 25 °C and nominal power-supply voltages. The complete receiver shows a system sensitivity of approximately -32.8 dBm with a bit error rate of  $1 \times 10^{-10}$ .

## Conclusion

A complete 2.5 Gbits/s SONET receiver has been described. The circuit shows that with careful attention to circuit design and printed-wiring board layout, performance exceeding all SONET requirements for sensitivity and jitter can be achieved.

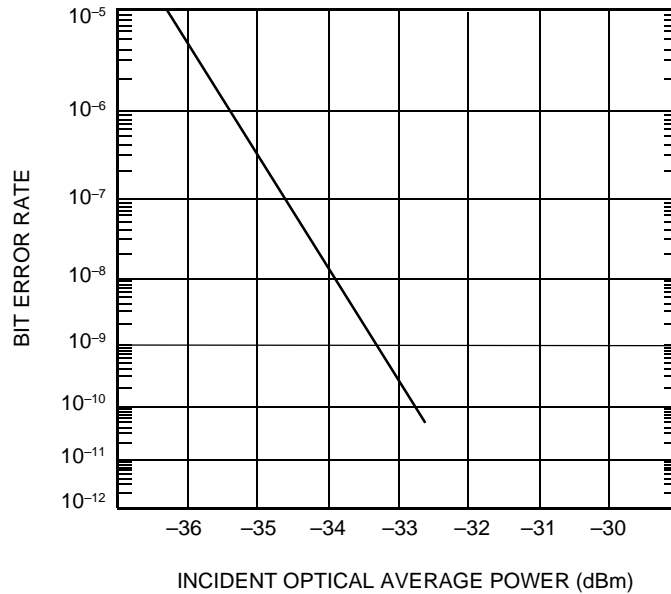


Figure 8. Complete Receiver BER Plot

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## Related Information

**Table 2. Related Product Information**

Description	Part Number	Document Number
High-Speed Lightwave Receiver	1319-Type	DS95-116LWP
2.5 Gbits/s Clock and Data Regenerator	LG1600FXH 2488	DS96-236FCE*
Limiting Amplifier 2.5 Gbits/s	LG1605DXB	DS96-237FCE*

\* For more information, call the Lucent Technologies Microelectronics Group customer hotline at 1-800-372-2447.

## References

“Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria,”  
*Bellcore GR-253-CORE*, Issue 1, December, 1994.

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For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: <http://www.lucent.com/micro>, or for Optoelectronics information, <http://www.lucent.com/micro/opto>  
E-MAIL: [docmaster@micro.lucent.com](mailto:docmaster@micro.lucent.com)  
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103  
**1-800-372-2447**, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)  
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256  
**Tel. (65) 778 8833**, FAX (65) 777 7495  
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road,  
Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468, ext. 316**, FAX (86) 21 6440 0652  
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan  
**Tel. (81) 3 5421 1600**, FAX (81) 3 5421 1700  
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1189 324 299**, FAX (44) 1189 328 148  
Technical Inquiries: OPTOELECTRONICS MARKETING: **(44) 1344 865 900** (Ascot UK)

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