Signetics

10192
Bus Driver

Quad Bus Driver
Product Specification

ECL Products

DESCRIPTION

The 10192 contains four line drivers with complementary outputs. Each driver has a Data (D_n) input and shares an Enable ($\overline{E}_n$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K ECL input signals and provides a nominal signal of 800mV across a 50Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage VLR does not cause an output collector to go more negative than −2.4V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5V with respect to V_{CC}. When the $\overline{E}_n$ input is HIGH, both output transistors of a driver are nonconducting. When not used, the $\overline{E}_n$ inputs, as well as the D_n inputs, may be left open.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT ($-I_{EE}$)
10192	3.0ns	110mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = GND; V_{EE} = −5.2V T_A = −30°C to +85°C
Plastic DIP	10192N
Ceramic DIP	10192F

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{E}_0$, $\overline{E}_1$	Enable Inputs
$Q_0 - Q_3$, $\overline{Q}_0 - \overline{Q}_3$	Data Outputs

PIN CONFIGURATION

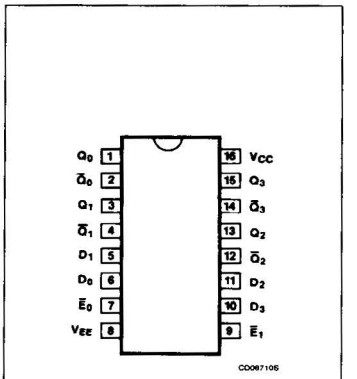


Figure 1

LOGIC SYMBOL

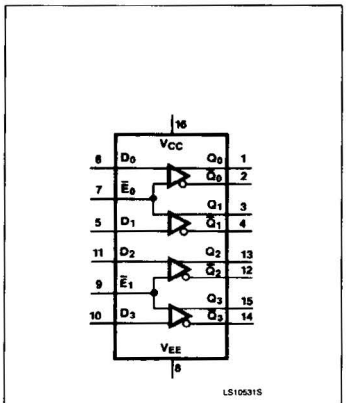
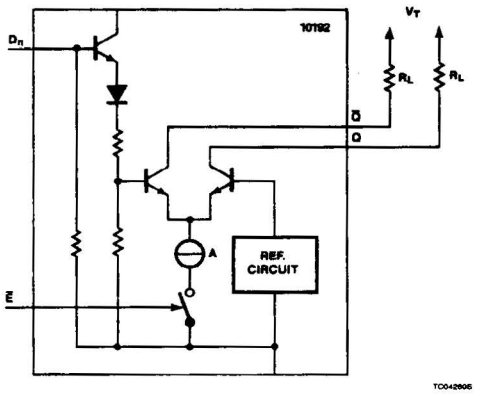


Figure 2



NOTES:
A = 16mA switched current source.
V_T should not exceed +5.5V and R_L and V_T should be chosen so that V_C does not go more negative than −2.4V.

Figure 3. Simplified Circuit Diagram

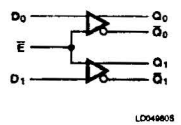


Figure 4. Logic Function

Basic driver operation
$V_{OH} = V_T$
$V_{OL} = V_T - 0.016 \cdot R_L$ (typ.)

FUNCTION TABLE

INPUTS		OUTPUTS			
		Current		Voltage	
$\overline{E}$	D	$\overline{Q}$	Q	$\overline{Q}$	Q
L	L	L	H	H	L
L	H	H	L	L	H
H	X	L	L	H	H

Positive Logic:
H (Voltage) = HIGH state (the more positive voltage) = 1
H (Current) = Output transistor not conducting (the least current flow)
L (Voltage) = LOW state (the more negative voltage) = 0
L (Current) = Output transistor conducting (the most current flow)
X = Don't Care
Z = High Impedance (Current source turned off)

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

PARAMETER			10K ECL	UNIT
V_{EE}	Supply voltage		−8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
V_T	Load termination voltage		5.5	V
V_O	Output voltage (at collector)	Max	+5.5	V
		Min	−2.4	V
T_S	Storage temperature		−55 to +150	°C
T_J	Maximum junction temperature	Ceramic package	+165	°C
		Plastic package	+150	°C

DC OPERATING CONDITIONS

PARAMETER			10K ECL			UNIT
			Min	Nom	Max	
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			−5.2		V
V_{IH}	HIGH level input voltage	T_A = −30°C			−890	mV
		T_A = +25°C			−810	mV
		T_A = +85°C			−700	mV
V_{IHT}	HIGH level input threshold voltage	T_A = −30°C	−1205			mV
		T_A = +25°C	−1105			mV
		T_A = +85°C	−1035			mV
V_{ILT}	LOW level input threshold voltage	T_A = −30°C			−1500	mV
		T_A = +25°C			−1475	mV
		T_A = +85°C			−1440	mV
V_{IL}	LOW level input voltage	T_A = −30°C	−1890			mV
		T_A = +25°C	−1850			mV
		T_A = +85°C	−1825			mV
T_A	Operating ambient temperature		−30	+25	+85	°C

NOTE:
When operating at V_{EE} other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

DC ELECTRICAL CHARACTERISTICS V_{CC} = GND, V_{EE} = −5.2V ±0.010V, T_A = −30°C to +85°C, output loading with 50Ω to V_T unless otherwise specified[1, 3]

PARAMETER			MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]
I_{OH}	Output current HIGH state	T_A = −30°C			2.0	mA	For $\overline{Q}$ outputs, apply V_{ILmin} to all inputs. For Q outputs, apply V_{ILmin} to $\overline{E}_n$ inputs with V_{IHmax} applied to D_n inputs.
		T_A = +25°C			2.0	mA	
		T_A = +85°C			2.0	mA	
I_{OHT}	Output threshold current HIGH state	T_A = −30°C				mA	For Q outputs, apply V_{IHT} to each D_n input, one at a time, with V_{ILmin} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{ILT} to each D_n input, one at a time, with V_{ILmin} applied to all other inputs.
		T_A = +25°C			2.0	mA	
		T_A = +85°C				mA	
I_{OLT}	Output threshold current LOW state	T_A = −30°C	13.5			mA	For Q outputs, apply V_{ILT} to each D_n input, one at a time, with V_{ILmin} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHT} to each D_n input, one at a time, with V_{ILmin} applied to all other inputs.
		T_A = +25°C	14			mA	
		T_A = +85°C	14			mA	
I_{OL}	Output current LOW state	T_A = −30°C	13.5		18	mA	For $\overline{Q}$ outputs, apply V_{IHmax} to D_n inputs with V_{ILmin} applied to $\overline{E}_n$ inputs. For Q outputs, apply V_{ILmin} to all inputs.
		T_A = +25°C	14		18	mA	
		T_A = +85°C	14		19	mA	
I_{OZ}	Output leakage current HIGH impedance	T_A = −30°C			300	µA	Apply V_{IHmax} to all inputs.
		T_A = +25°C			300	µA	
		T_A = +85°C			300	µA	
I_{IH}	HIGH level input current	T_A = −30°C			425	µA	Apply V_{IHmax} to each input under test, one at a time, with V_{ILmin} applied to all other inputs.
		T_A = +25°C			265	µA	
		T_A = +85°C			265	µA	
I_{IL}	LOW level input current	T_A = −30°C	0.5			µA	Apply V_{ILmin} to each input under test, one at a time, with V_{IHmax} applied to all other inputs.
		T_A = +25°C	0.5			µA	
		T_A = +85°C	0.3			µA	
$-I_{EE}$	V_{EE} supply current	T_A = −30°C			154	mA	
		T_A = +25°C		110	140	mA	
		T_A = +85°C			154	mA	
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	HIGH level output voltage compensation	T_A = +25°C		0.016		V/V	
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	LOW level output voltage compensation			0.250		V/V	
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V	

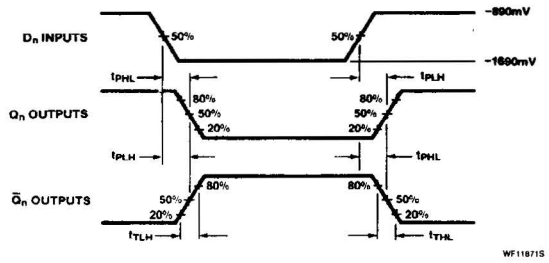
NOTES:

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 0V (GND), V_{EE} = −5.2V ±0.010V, V_T = GND (0V)

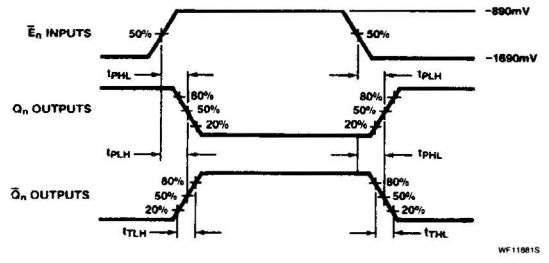
PARAMETER		T_A = 30°C		T_A = +25°C			T_A = +85°C		UNIT	TEST CONDITIONS
		Min	Max	Min	Typ	Max	Min	Max		
t_{PLH}	Propagation delay	2.0	4.7	2.0	3.0	4.5	2.0	4.8	ns	Figs. 5, 7, 8
t_{PHL}	D_n to Q_n, $\overline{Q}_n$	2.0	4.7	2.0	3.0	4.5	2.0	4.8	ns	
t_{PLH}	Propagation delay	2.5	6.3	2.5	3.5	6.0	2.5	6.6	ns	Figs. 6, 7, 8
t_{PHL}	$\overline{E}_n$ to Q_n, $\overline{Q}_n$	2.5	6.3	2.5	3.5	6.0	2.5	6.6	ns	
t_{TLH}	Transition time	1.3	3.5	1.3	2.3	3.3	1.3	3.5	ns	Figs. 5, 6, 7, 8
t_{THL}	20% to 80%, 80% to 20%	1.3	3.5	1.3	2.3	3.3	1.3	3.5	ns	

AC WAVEFORMS



NOTE:
Output waveforms represent voltage across load resistor (R_L)

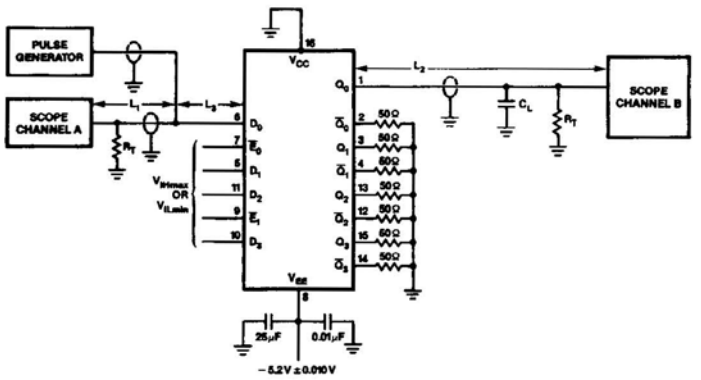
Figure 5. Propagation Delay and Transition Times for Data to Outputs



NOTE:
Output waveforms represent voltage across load resistor (R_L).

Figure 6. Propagation Delay and Transition Times for Enable to Outputs

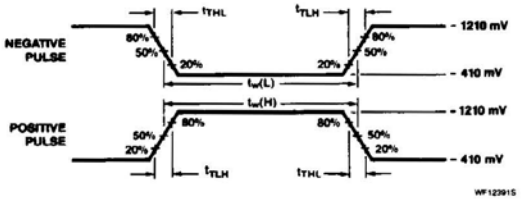
TEST CIRCUITS AND WAVEFORMS



NOTES:

1. $V_{CC1} = V_{CC2} = GND$ (0V), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE} (0.01μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $< 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10192



INPUT PULSE REQUIREMENTS $V_{CC1} = GND$ (0V), $V_{EE} = -5.2V \pm 0.010V$, $V_T = GND$ (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
10K ECL	800mVp-p	1MHz	500ns	2.0 ±0.2ns	2.0 ±0.2ns

Figure 8. Input Pulse Definition

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