Signetics

10136
Universal Counter

Universal Hexadecimal Counter
Product Specification

ECL Products

DESCRIPTION

The 10136 is a high-speed Hexadecimal Synchronous Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The operation mode of the counter is programmed by three control lines (S_0, S_1, and CP) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2, and D_3) to be entered into the counter. $\overline{C}_{out}$ goes LOW on the terminal count, or when the counter is being preset.

The counter changes state only on the positive-going edge of the clock, so at any other time any other input may change without any result (except for $\overline{C}_{out}$).

This binary counter can be used in many applications, such as in computing for high-speed control processors and peripheral controllers. Unused inputs must be tied LOW to V_{IL} or V_{EE}.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT ($-I_{EE}$)
10136	3.3ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$
Plastic DIP	10136N
Ceramic DIP	10136F

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$\overline{C}_{in}$	Carry-in Input
S_0, S_1	Select Inputs
$\overline{C}_{out}$	Carry-out Output
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION

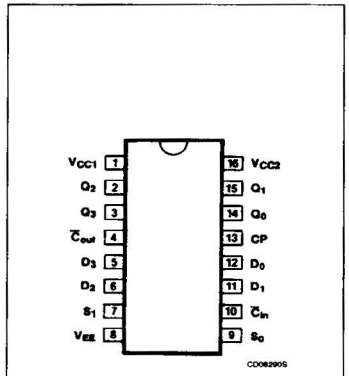


Figure 1

LOGIC SYMBOL

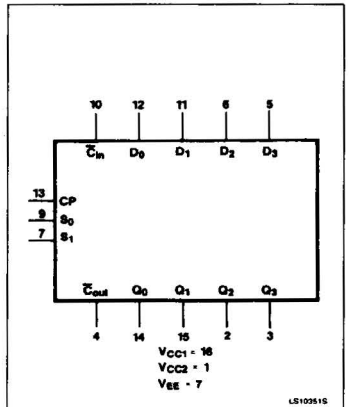


Figure 2

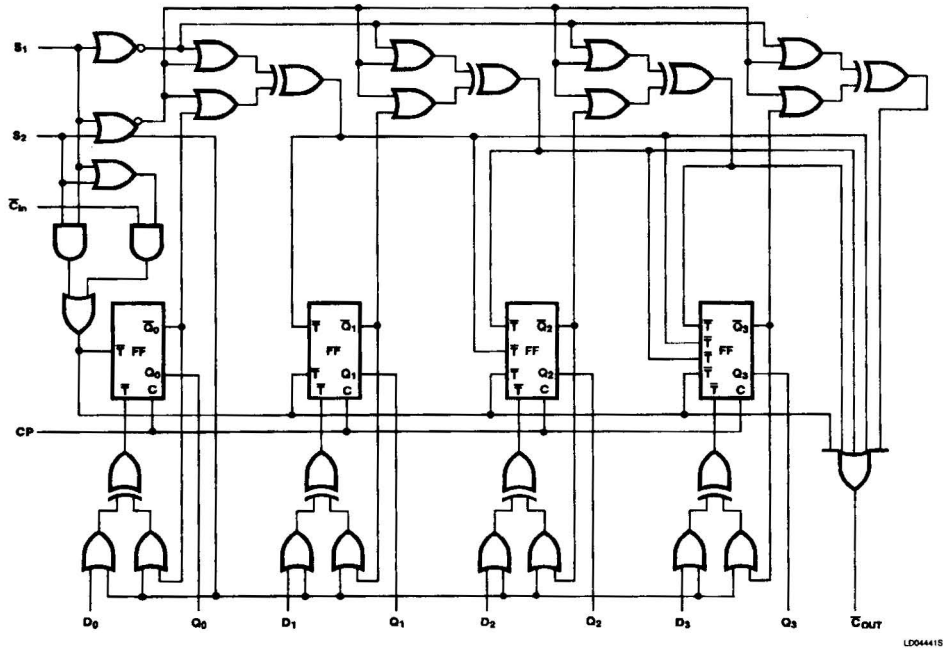


Figure 3. Logic Diagram

FUNCTION SELECT TABLE

S_0	S_1	OPERATING MODE
L	L	Preset (program)
L	H	Increment (count up)
H	L	Decrement (count down)
H	H	Hold (stop count)

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

SEQUENTIAL FUNCTION TABLE

INPUTS								OUTPUTS				
S_0	S_1	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	CP	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

PARAMETER			10K ECL	UNIT
V_{EE}	Supply voltage		−8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current		−50	mA
T_S	Storage temperature		−55 to +150	°C
T_J	Maximum junction temperature	Ceramic package	+165	°C
		Plastic package	+150	°C

DC OPERATING CONDITIONS

PARAMETER			10K ECL			UNIT
			Min	Nom	Max	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			−5.2		V
V_{IH}	HIGH level input voltage	T_A = −30°C			−890	mV
		T_A = +25°C			−810	mV
		T_A = +85°C			−700	mV
V_{IHT}	HIGH level input threshold voltage	T_A = −30°C	−1205			mV
		T_A = +25°C	−1105			mV
		T_A = +85°C	−1035			mV
V_{ILT}	LOW level input threshold voltage	T_A = −30°C			−1500	mV
		T_A = +25°C			−1475	mV
		T_A = +85°C			−1440	mV
V_{IL}	LOW level input voltage	T_A = −30°C	−1890			mV
		T_A = +25°C	−1850			mV
		T_A = +85°C	−1825			mV
T_A	Operating ambient temperature		−30	+25	+85	°C

NOTE:
When operating at V_{EE} other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

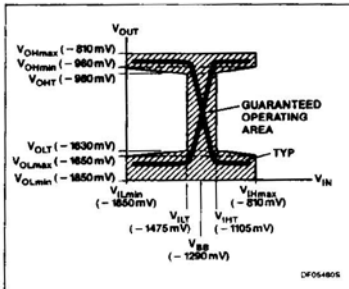
PARAMETER				MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]
V_{OH}	HIGH level output voltage		$T_A = -30°C$	-1060		-890	mV	Apply V_{IHmax} to all inputs.
			$T_A = +25°C$	-960		-810	mV	
			$T_A = +85°C$	-890		-700	mV	
V_{OHT}	HIGH level output threshold voltage		$T_A = -30°C$	-1080			mV	Apply V_{IHT} to each input, one at a time, with V_{IHmax} applied to all other inputs.
			$T_A = +25°C$	-980			mV	
			$T_A = +85°C$	-910			mV	
V_{OLT}	LOW level output threshold voltage		$T_A = -30°C$			-1655	mV	Apply V_{IHT} to S_0 input with V_{IHmax} applied to CP input and V_{ILmin} applied to all other inputs.
			$T_A = +25°C$			-1630	mV	
			$T_A = +85°C$			-1595	mV	
V_{OL}	LOW level output voltage		$T_A = -30°C$	-1890		-1675	mV	Apply V_{IHmax} to S_0 and CP inputs with V_{ILmin} applied to all other inputs.
			$T_A = +25°C$	-1850		-1650	mV	
			$T_A = +85°C$	-1825		-1615	mV	
I_{IH}	HIGH level input current	D_n inputs	$T_A = -30°C$			350	µA	Apply V_{IHmax} to each input under test, one at a time, with V_{ILmin} applied to all other inputs.
			$T_A = +25°C$			220	µA	
			$T_A = +85°C$			220	µA	
		S_1 input	$T_A = -30°C$			425	µA	
			$T_A = +25°C$			265	µA	
			$T_A = +85°C$			265	µA	
		S_0, $\overline{C}_{in}$ inputs	$T_A = -30°C$			390	µA	
			$T_A = +25°C$			245	µA	
			$T_A = +85°C$			245	µA	
		CP input	$T_A = -30°C$			460	µA	Apply V_{IHmax} to CP input with V_{ILmin} applied to all other inputs.
			$T_A = +25°C$			290	µA	
			$T_A = +85°C$			290	µA	
I_{IL}	LOW level input current		$T_A = -30°C$	0.5			µA	Apply V_{ILmin} to each input under test, one at a time, with V_{IHmax} applied to all other inputs.
			$T_A = +25°C$	0.5			µA	
			$T_A = +85°C$	0.3			µA	
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$			165	mA	
			$T_A = +25°C$		120	150	mA	
			$T_A = +85°C$			165	mA	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS[2]
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$ HIGH level output voltage compensation	$T_A = +25°C$		0.016		V/V	
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$ LOW level output voltage compensation			0.250		V/V	
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$ Reference bias voltage compensation			0.148		V/V	

NOTES:

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



NOTES:

V_{IHmax} – Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} – HIGH level input threshold voltage.
V_{ILT} – LOW level input threshold voltage.
V_{ILmin} – Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHmax} – Maximum HIGH level output voltage (the most positive V_{OH}) under the specified input and loading condition.
V_{OHmin} – Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OHT} – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLT} – LOW level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLmax} – Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{OLmin} – Minimum LOW level output voltage (the most negative V_{OL}) under the specified input and loading conditions.
V_{BB} – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 4. Transfer Characteristics

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

PARAMETER		$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		UNIT	TEST CONDITIONS
		Min	Max	Min	Typ	Max	Min	Max		
f_{MAX}	Maximum clock frequency	125		125	150		125		MHz	Figs. 5, 10, 11
t_{PLH}	Propagation delay CP to Q_n	1.7 1.7	4.8 4.8	1.7 1.7	3.3 3.3	4.5 4.5	1.7 1.7	5.0 5.0	ns ns	Figs. 5, 6, 7, 10, 11
t_{PHL}	Propagation delay CP to $\overline{C}_{OUT}$	2.0 2.0	10.9 10.9	2.5 2.5	7.0 7.0	10.5 10.5	2.4 2.4	11.5 11.5	ns ns	
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$	1.6 1.6	7.4 7.4	1.6 1.6	5.0 5.0	6.9 6.9	1.9 1.9	7.5 7.5	ns ns	
t_s	Setup time D_n to CP	3.5		3.5			3.5		ns	Figs. 8, 10, 11
t_h	Hold time D_n to CP	0.0		0.0			0.0		ns	
t_s	Setup time S_n to CP	7.5		7.5			7.5		ns	
t_h	Hold time S_n to CP	−2.5		−2.5			−2.5		ns	
t_s	Setup time $\overline{C}_{IN}$ to CP CP to $\overline{C}_{IN}$	4.5 −1.0		3.7 −1.0			4.5 −1.0		ns ns	Figs. 9, 10, 11
t_h	Hold time CP to $\overline{C}_{IN}$ $\overline{C}_{IN}$ to CP	−1.6 4.0		−1.6 3.1			−1.6 4.0		ns ns	
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	ns ns	Figs. 5, 6, 7, 10, 11

AC WAVEFORMS

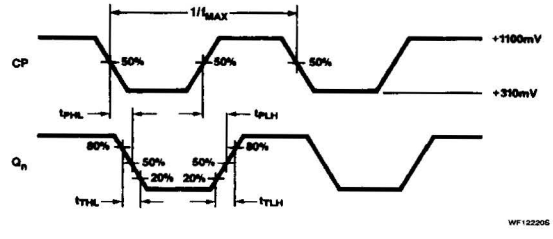


Figure 5. Propagation Delay and Transition Times for Clock Input to Outputs and Maximum Clock Frequency

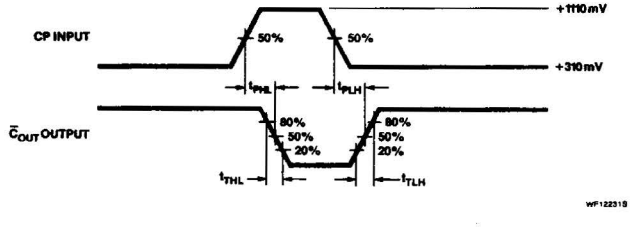
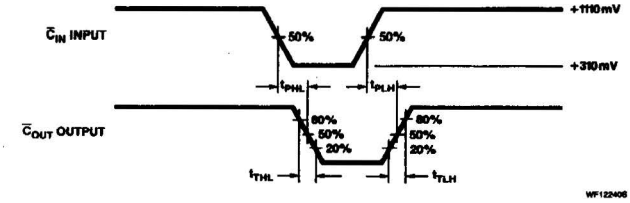


Figure 6. Propagation Delay and Transition Time for Clock Input to Carry-Out Output



NOTE:
Setup times are the minimum times before the positive transition of the clock pulse (CP) that information must be present at the data input (D) or control input (S).
Hold times are the minimum times after the positive transition of the clock pulse (CP) that information must remain unchanged at the data input (D) or control input (S).

Figure 7. Propogation Delay and Transtion Time for Carry-In Input to Carry-Out Output

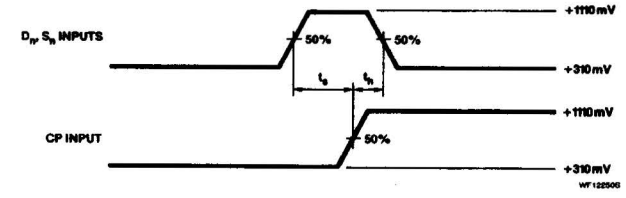
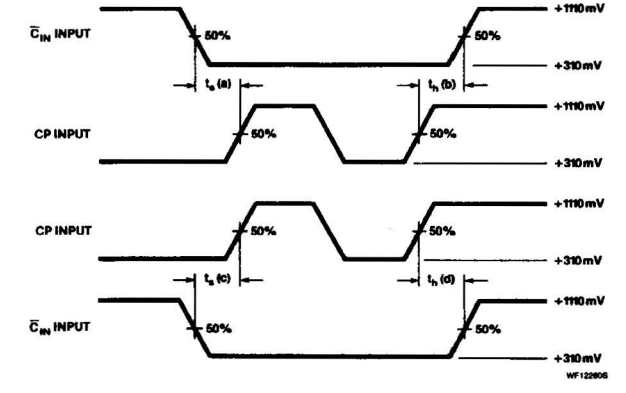


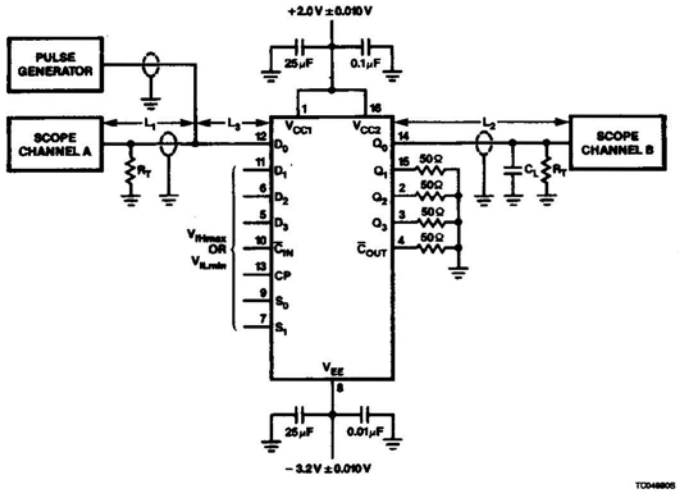
Figure 8. Setup and Hold Times for Data And Select Inputs to Clock Input



NOTE:
(a) is the minimum time to wait to clock the counter after it has been enabled.
(b) is the minimum time that the counter may be clocked before it has been disabled.
(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.
(b) and (c) may be negative numbers.

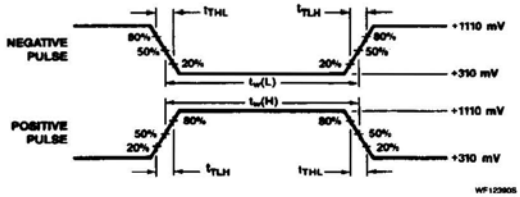
Figure 9. Setup and Hold Times for Carry-In to Clock Input

TEST CIRCUITS AND WAVEFORMS



NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 10. Test Circuit



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, V_T = GND (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
10K ECL	800mVp-p	1MHz	500ns	2.0 ±0.2ns	2.0 ±0.2ns

Figure 11. Input Pulse Definition