

100363

Low Power Dual 8-Input Multiplexer

General Description

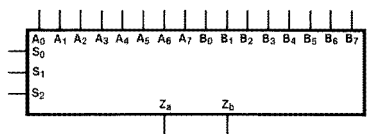
The 100363 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b , respectively). The same bit (0–7) will be selected for both the Z_a and Z_b output. All inputs have 50 k Ω pulldown resistors.

- 2000V ESD protection
- Pin/function compatible with 100163
- Voltage compensated operating range = -4.2V to -5.7V
- Standard Microcircuit Drawing (SMD) 5962-9165501

Features

- 50% power reduction of the 100163

Logic Symbol

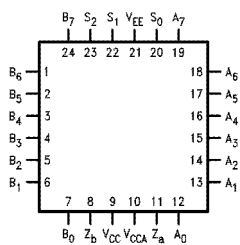


DS100310-1

| Pin Names | Description |
|---------------|--------------------|
| S_0 - S_2 | Data Select Inputs |
| A_0 - A_7 | A Data Inputs |
| B_0 - B_7 | B Data Inputs |
| Z_a , Z_b | Data Outputs |

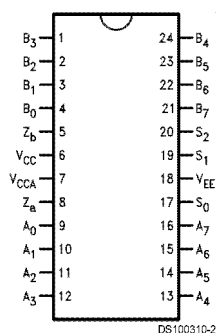
Connection Diagrams

24-Pin Quad Cerpak



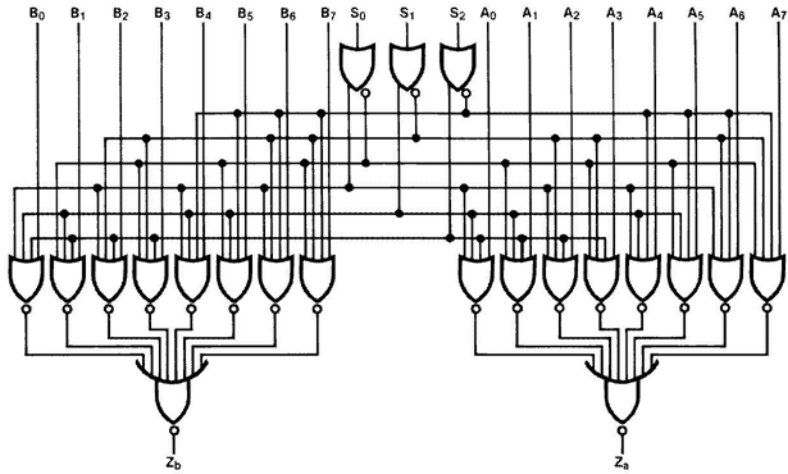
DS100310-3

24-Pin DIP



DS100310-2

Logic Diagram



DS100310-5

Truth Table

| Select | | | Inputs | | | | | | | | Outputs | |
|----------------|----------------|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------|----------------|
| S ₂ | S ₁ | S ₀ | Data | | | | | | | | Z _a | Z _b |
| | | | A ₇ B ₇ | A ₆ B ₆ | A ₅ B ₅ | A ₄ B ₄ | A ₃ B ₃ | A ₂ B ₂ | A ₁ B ₁ | A ₀ B ₀ | | |
| L | L | L | | | | | | | | | L | L |
| L | L | L | | | | | | | | | H | H |
| L | L | H | | | | | | | | L | | L |
| L | L | H | | | | | | | | H | | H |
| L | H | L | | | | | | | L | | | L |
| L | H | L | | | | | | | H | | | H |
| L | H | H | | | | | | L | | | | L |
| L | H | H | | | | | | H | | | | H |
| H | L | L | | | | L | | | | | | L |
| H | L | L | | | | H | | | | | | H |
| H | L | H | | | L | | | | | | | L |
| H | L | H | | | H | | | | | | | H |
| H | H | L | | L | | | | | | | | L |
| H | H | L | | H | | | | | | | | H |
| H | H | H | L | | | | | | | | | L |
| H | H | H | H | | | | | | | | | H |

H = HIGH Voltage Level

L = LOW Voltage Level

Blank = X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

| | |
|--|--------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to + 0.5V |
| Output Current (DC Output HIGH) | -50 mA |

ESD (Note 2)

≥2000V

Recommended Operating Conditions

Case Temperature (T_C)

Military -55°C to +125°C

Supply Voltage (V_{EE})

-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Note | |
|-----------|----------------------|------------|-------|-------|-----------------|--|---------------------------|-----------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | 0°C to +125°C | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to -2.0V | (Notes 3, 4, 5) |
| | | -1085 | -870 | mV | -55°C | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | 0°C to +125°C | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to -2.0V | (Notes 3, 4, 5) |
| | | -1830 | -1555 | mV | -55°C | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | 0°C to +125°C | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to -2.0V | (Notes 3, 4, 5) |
| | | -1085 | | mV | -55°C | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | 0°C to +125°C | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to -2.0V | (Notes 3, 4, 5) |
| | | | -1555 | mV | -55°C | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | -55°C to +125°C | Guaranteed HIGH Signal for All Inputs | (Notes 3, 4, 5, 6) | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | -55°C to +125°C | Guaranteed LOW Signal for All Inputs | (Notes 3, 4, 5, 6) | |
| I_{IL} | Input LOW Current | 0.50 | | μA | -55°C to +125°C | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | (Notes 3, 4, 5) | |
| I_{IH} | Input HIGH Current | S_n | 265 | μA | 0°C to +125°C | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | (Notes 3, 4, 5) | |
| | | A_n, B_n | 340 | μA | -55°C | | | |
| I_{IH} | Input HIGH Current | S_n | 385 | μA | -55°C | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | (Notes 3, 4, 5) | |
| | | A_n, B_n | 490 | μA | -55°C | | | |
| I_{EE} | Power Supply Current | -87 | -30 | mA | -55°C to +125°C | Inputs Open | (Notes 3, 4, 5) | |

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table 1) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

| Symbol | Parameter | $T_C = -55^\circ\text{C}$ | | $T_C = +25^\circ\text{C}$ | | $T_C = +125^\circ\text{C}$ | | Units | Conditions | Notes |
|-----------|---|---------------------------|------|---------------------------|------|----------------------------|------|-------|--------------------------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} | Propagation Delay | 0.50 | 2.40 | 0.60 | 2.30 | 0.70 | 3.00 | ns | Figure 1 and Figure 2 | (Notes 7, 8, 9) |
| t_{PHL} | A_0 - A_7 , B_0 - B_7 to Output | | | | | | | | | |
| t_{PLH} | Propagation Delay | 0.80 | 3.00 | 0.90 | 2.80 | 0.80 | 3.40 | ns | | |
| t_{PHL} | S_0 - S_2 to Output | | | | | | | | | |
| t_{TLH} | Transition Time | 0.30 | 1.90 | 0.30 | 1.80 | 0.30 | 2.10 | ns | | (Note 10) |
| t_{THL} | 20% to 80%, 80% to 20% | | | | | | | | | |

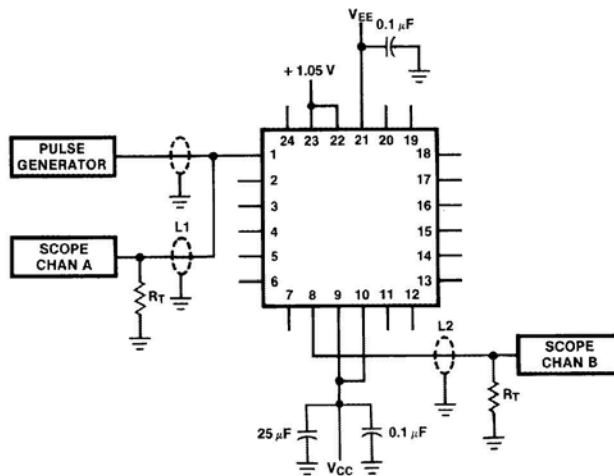
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ\text{C}$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ\text{C}$, Subgroup A9, and at $+125^\circ\text{C}$ and -55°C , temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C temperature (design characterization data).

Test Circuitry



DS100310-6

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

$L1$ and $L2$ = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1 \mu\text{F}$ from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance $\leq 3 \text{ pF}$

Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Switching Waveforms

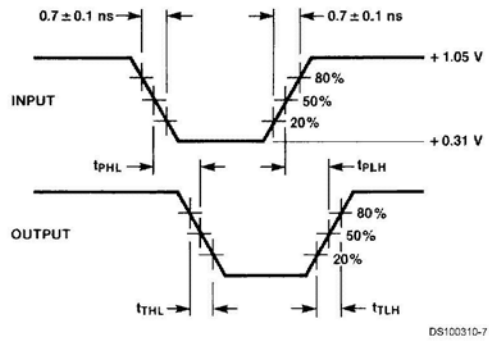
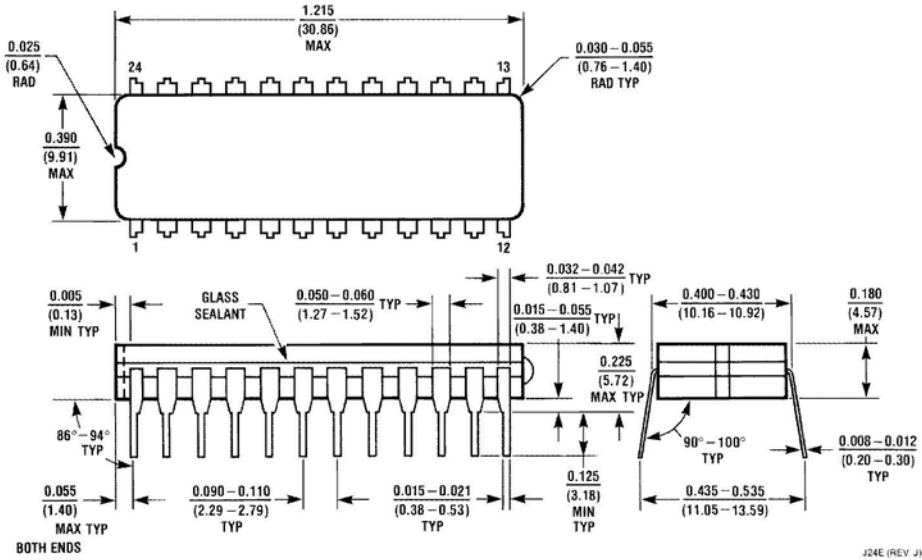
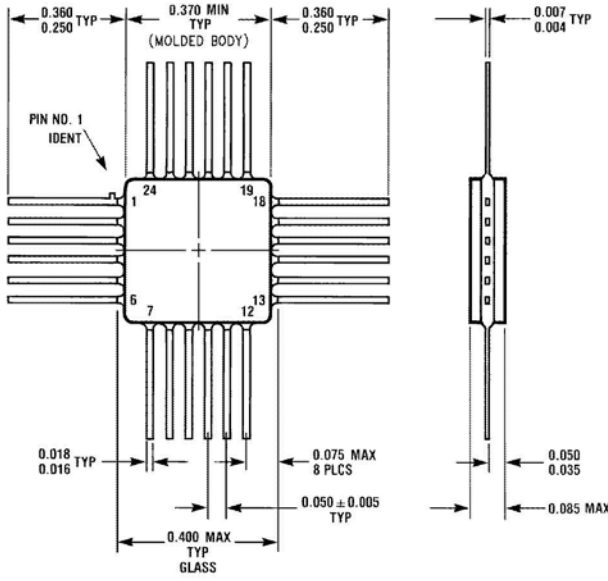


FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Pin Quad Cerpak (F)
NS Package Number W24B

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