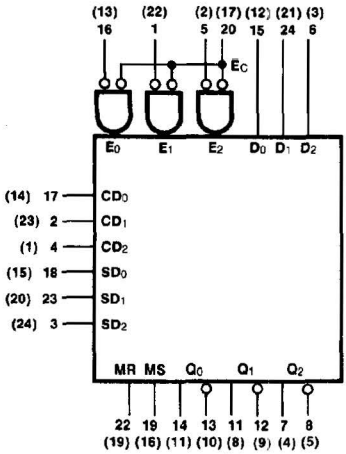
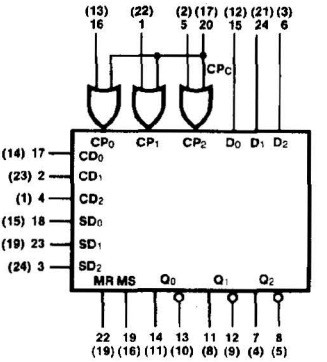
DIGITAL-ECL

E45
100130



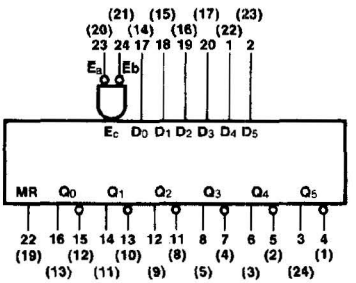
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

E46
100131



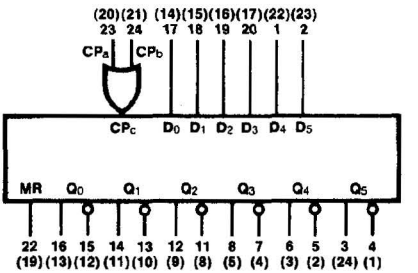
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

E47
100150



V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

E48
100151



V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

ECL

LATCHES/FLIP-FLOPS (Cont'd)

Item	Function	DEVICE NO.*	Data Inputs	Direct Set/Clear or Common Clear	Enable/Clock Inputs (Level)	Required Enable/Clock Pulse Width-ns (Typ)	Enable /Clock to Q Delay-ns (Typ)	Data to Q Delay ns (Typ)	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
1	Hex D Flip-Flop	**10186/10586**	6	Yes	⎍	3.0	3.0	5.0	455	E41	4L,6B,9B
2	Hex D Flip-Flop	**100151**	6	Yes	⎍	1.4	1.1	0.75	550	E48	4Q,6Q
3	Master/Slave D Flip-Flop	**11C70**	1	Yes	⎍	0.7	1.0	1.0	210	E44	6B
4	JK Flip-Flop	**95H29**	1	Yes	⎍	2.0	3.0	3.0	180	E27	6B
5	JK Flip-Flop	**95029**	3	Yes	⎍	2.0	2.8	2.8	185	E29	6B
6	Dual JK Flip-Flop	**10135/10535**	2	No	⎍	2.5	3.0	3.0	235	E35	4L,6B,9B
7	Dual D Latch	**95130**	2	Yes	H	2.5	2.7	2.5	135	E30	6B
8	Dual D Latch	**10130/10530**	2	Yes	H	2.5	2.7	2.5	135	E30	4L,6B,9B
9	Triple D Latch	**100130**	3	Yes	H	1.0	1.3	0.85	400	E45	4Q,6Q
10	Quad Latch	**9534**	4	Yes	L	2.2	5.6	4.3	415	E28	6B
11	Quad Latch	**10133/10533**	4	No	L	4.0	4.0	4.0	310	E33	4L,6B,9B
12	Quad Latch	**10153/10553**	4	No	H	4.0	4.0	4.0	310	E36	4L,6B,9B
13	Quad Latch	**10168/10568**	4	No	L	4.0	4.0	4.0	310	E39	4L,6B,9B
14	Quint Latch	**10175/10575**	5	Yes	H	3.3	3.3	2.5	405	E49	4L,6B,9B
15	Hex D Latch	**100150**	6	Yes	H	1.4	1.1	0.75	420	E37	4Q,6Q
16	Dual Mux/Latch	**10132/10532**	4	Yes	H	4.5	4.5	3.5	230	E32	4L,6B,9B
17	Dual Mux/Latch	**10134/10534**	4	No	H	4.6	4.5	3.0	230	E34	4L,6B,9B
18	Quad Mux/Latch	**10173/10573**	8	No	H	4.5	4.5	2.5	310	E38	4L,6B,9B
19	Quad Mux/Latch	**100155**	4+4	Yes	H	1.2	1.2	0.85	430	E47	4Q,6Q

*105XX and 106XX = Military temperature range