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ECL Products	

# 100124/100124A

## Hex TTL-to-ECL Translator

### FEATURES

- Typical propagation delay: 1.70ns
- Typical ECL supply current ( $-I_{EE}$ ): 96mA for the 100124 and 71mA for the 100124A
- Typical TTL supply current ( $I_{TTL}$ ): 44mA for the 100124 and 10mA for the 100124A

### DESCRIPTION

The 100124 is a hex translator that converts TTL logic levels to 100K ECL logic levels. When the common Enable (E) is Low, all true outputs are Low, and all inverting outputs are High. The differential outputs allow each circuit to be used as an inverting, noninverting, or differential line driver.

In differential operation, common mode rejection helps overcome ground offsets

and transients between the 100124 and its receiver.  $V_{EE}$  and  $V_{TTL}$  may be applied in any order.

The 100124A is a low power version of the 100124. The only difference between the two parts are the limits of the ECL and TTL supply currents.

All unused inputs can be left open due to integrated pull-down resistors.

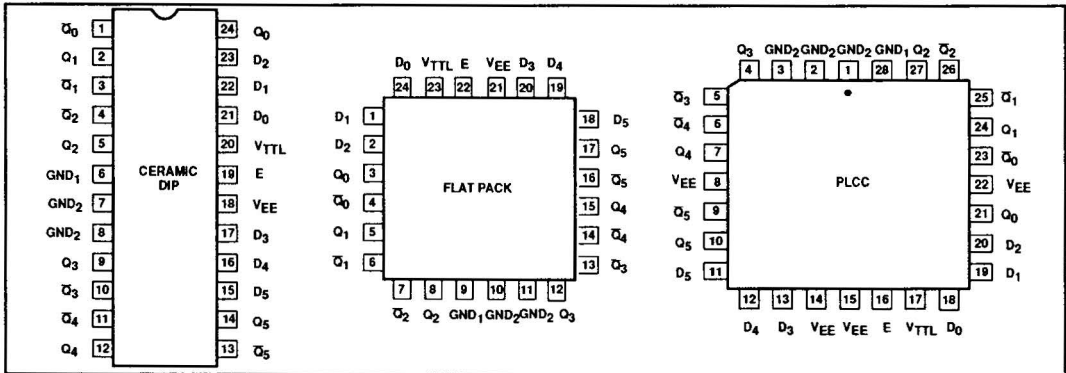
### PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs (TTL compatible)
E	Enable input (TTL compatible)
$Q_0 - Q_5$	True data outputs (100K ECL compatible)
$\bar{Q}_0 - \bar{Q}_5$	Complementary data outputs (100K ECL compatible)

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP (400 mils wide)	100124F/100124AF
24-Pin Ceramic Flat Pack	100124Y/100124AY
28-Pin PLCC	100124A/100124AA

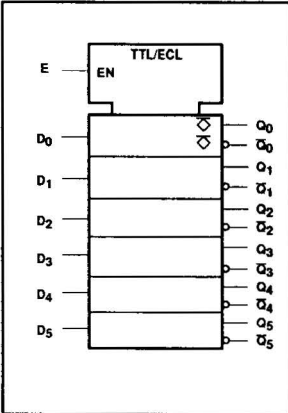
### PIN CONFIGURATIONS



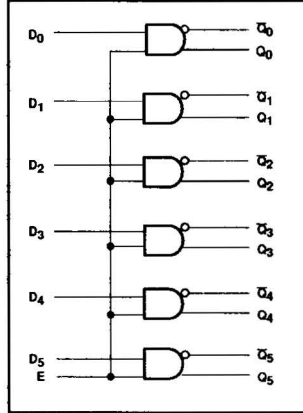
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### IEC/IEEE SYMBOL



### LOGIC DIAGRAM

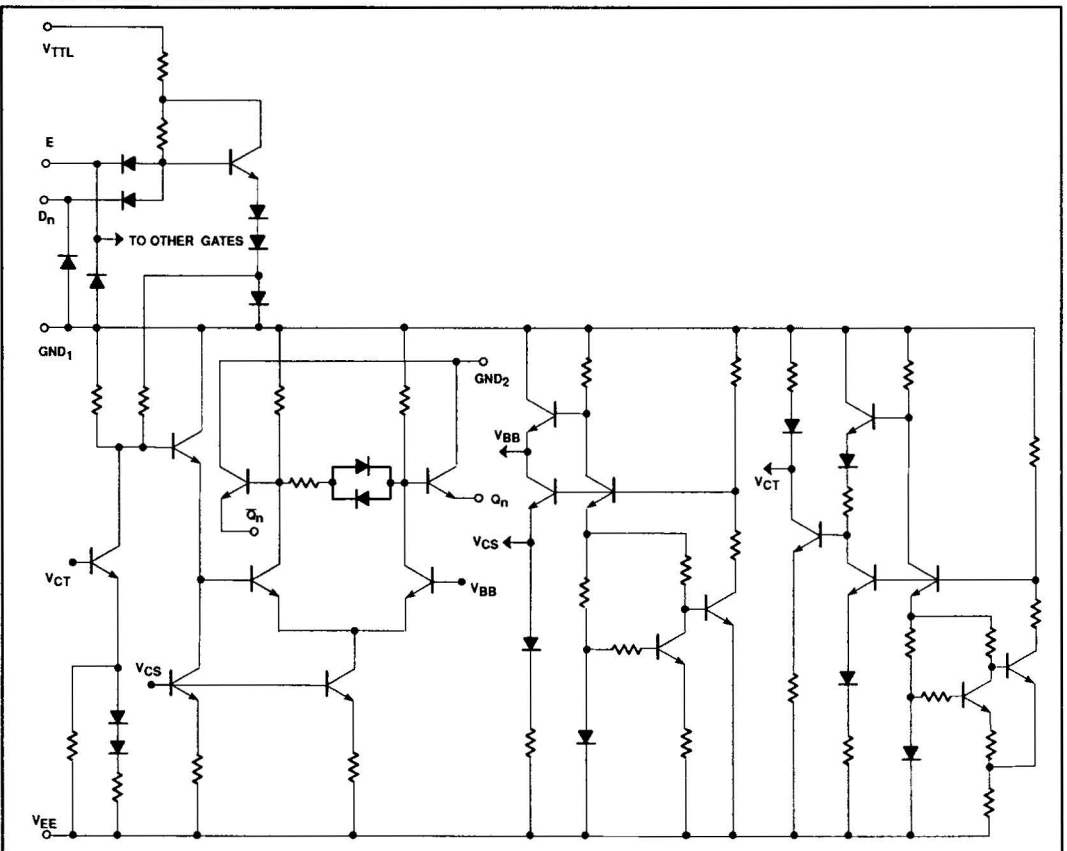


### FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
E	D <sub>n</sub>	Q <sub>n</sub>	$\bar{Q}_n$
H	H	H	L
H	L	L	H
L	X	L	H

NOTES:  
 H = High voltage level  
 L = Low voltage level  
 X = Don't care

### SIMPLIFIED SCHEMATIC



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**ABSOLUTE MAXIMUM RATINGS**  $GND_1 = GND_2 = \text{ground}$ ,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
$V_{TTL}$	TTL Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to $V_{TTL}$	V
$I_{IN}$	Input current	-30 to +5.0	mA
$V_{EE}$	ECL Supply voltage	-7.0 to +0.5	V
$I_O$	Output source current (continuous)	-55	mA
$T_S$	Storage temperature range	-65 to +150	$^\circ\text{C}$
$T_J$	Maximum junction temperature	+150	$^\circ\text{C}$

**NOTE:**

Operation beyond the limits set forth in this table may impair the useful life of the device.

**DC OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
$GND_1, GND_2$	Circuit ground	0	0	0	V
$V_{TTL}$	TTL Supply voltage	+4.5	+5.0	+5.5	V
$V_{EE}$	ECL Supply voltage	-4.8	-4.5	-4.2	V
$V_{EE}$	Supply voltage when operating with the 10K or the 10KH ECL family	-5.7			V
$V_{IH}$	High level input voltage	+2.0			V
$V_{IL}$	Low level input voltage			+0.8	V
$T_A$	Operating ambient temperature range	0	+25	+85	$^\circ\text{C}$

**NOTE:**When operating at other than the  $V_{EE}$  specified voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

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**DC ELECTRICAL CHARACTERISTICS**  $GND_1 = GND_2 = \text{ground}$ ,  $V_{TTL} = 4.5\text{V to } 5.5\text{V}$ ,  $V_{EE} = -4.8\text{V to } -4.2\text{V}$ ,  $T_A = 0^\circ\text{C to } +85^\circ\text{C}$   
 unless otherwise specified<sup>1,3,4</sup>

SYMBOL	PARAMETER	TEST CONDITIONS <sup>2</sup>			LIMITS			UNIT	
					MIN.	TYP.	MAX.		
$V_{OH}$	High level output voltage	Outputs Loaded with $50\Omega$ to $-2.0\text{V}$ $\pm 0.010\text{V}$	E, $D_n = 2.4\text{V}$ , test $Q_n$	$V_{EE} = -4.2\text{V}$	-1020		-870	mV	
				$V_{EE} = -4.5\text{V}$	-1025	-955	-880	mV	
				$V_{EE} = -4.8\text{V}$	-1035		-880	mV	
$V_{OHT}$	High level output threshold voltage		E, $D_n = 2.0\text{V}$ , test $Q_n$	$V_{EE} = -4.2\text{V}$	-1030			mV	
				$V_{EE} = -4.5\text{V}$	-1035			mV	
				$V_{EE} = -4.8\text{V}$	-1045			mV	
$V_{OLT}$	Low level output threshold voltage		E, $D_n = 0.8\text{V}$ , test $Q_n$	$V_{EE} = -4.2\text{V}$			-1595	mV	
				$V_{EE} = -4.5\text{V}$			-1610	mV	
				$V_{EE} = -4.8\text{V}$			-1610	mV	
$V_{OL}$	Low level output voltage	E, $D_n = 0.4\text{V}$ , test $Q_n$	$V_{EE} = -4.2\text{V}$	-1810		-1605	mV		
			$V_{EE} = -4.5\text{V}$	-1810	-1705	-1620	mV		
			$V_{EE} = -4.8\text{V}$	-1830		-1620	mV		
$-I_{EE}$	$V_{EE}$ supply current	100124	All inputs $\geq V_{IHMIN}$			96	140	mA	
		100124A				71	90	mA	
$V_{IK}$	Input clamp voltage	$D_n$ inputs	Apply $-18\text{mA}$ to one $D_n$ , other inputs open.			-1.5		V	
		E input	Apply $-18\text{mA}$ to one E, other inputs open.			-1.5		V	
$I_I$	Input current at maximum input voltage	$D_n$ inputs	$D_n$ input under test $= +5.5\text{V}$ , other inputs = ground.				1.0	mA	
		E input	E = $+5.5\text{V}$ , other inputs = ground.				1.0	mA	
$I_{IH}$	High level input current	$D_n$ inputs	$D_n$ input under test $= +2.4\text{V}$ , other inputs = ground.				20	$\mu\text{A}$	
		E input	E = $+2.4\text{V}$ , other inputs = ground.				120	$\mu\text{A}$	
$-I_{IL}$	Low level input current	$D_n$ inputs	$D_n$ input under test $= +0.4\text{V}$ , other inputs = $+2.4\text{V}$ .				1.6	mA	
		E input	E = $+0.4\text{V}$ , other inputs = $+2.4\text{V}$ .				9.6	mA	
$I_{TTL}$	TTL supply current	100124	All inputs at ground.				44	75	mA
		100124A					10	15	mA

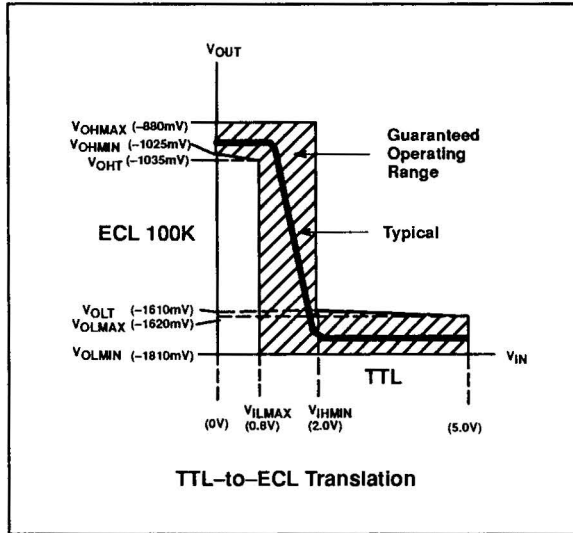
**NOTES:**

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- The device can function down to  $V_{EE} = -5.7\text{V}$ , allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended  $V_{EE}$  range. For more information, see Chapters 5 and 10, Section 4.

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## TRANSFER CHARACTERISTICS



## AC ELECTRICAL CHARACTERISTICS

Ceramic DIP  $GND_1 = GND_2 = \text{ground}$ ,  $V_{TTL} = 4.5V \text{ to } 5.5V$ ,  $V_{EE} = -4.8V \text{ to } -4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $D_n$ or $E$ to $Q_n$ or $\bar{Q}_n$	Waveform 1	0.50	3.00	0.50	2.90	0.50	3.00	ns
			0.50	3.00	0.50	2.90	0.50	3.00	ns
$t_{TLH}$ $t_{THL}$	Transition time $Q_n$ or $\bar{Q}_n$		0.45	1.80	0.45	1.80	0.45	1.80	ns
			0.45	1.80	0.45	1.80	0.45	1.80	ns

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC ELECTRICAL CHARACTERISTICS

Ceramic DIP  $GND_1 = GND_2 = \text{ground}$ ,  $V_{TTL} = 4.5V \text{ to } 5.5V$ ,  $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $D_n$ or $E$ to $Q_n$ or $\bar{Q}_n$	Waveform 1	0.50	3.00	0.50	2.90	0.50	3.00	ns
			0.50	3.00	0.50	2.90	0.50	3.00	ns
$t_{TLH}$ $t_{THL}$	Transition time $Q_n$ or $\bar{Q}_n$		0.45	1.80	0.45	1.80	0.45	1.80	ns
			0.45	1.80	0.45	1.80	0.45	1.80	ns

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

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## AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC  $GND_1 = GND_2 = \text{ground}$ ,  $V_{TTL} = 4.5\text{V to } 5.5\text{V}$ ,  $V_{EE} = -4.8\text{V to } -4.2\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $D_n$ or $E$ to $Q_n$ or $\bar{Q}_n$	Waveform 1	0.50	2.80	0.50	2.70	0.50	2.80	ns
0.50			2.80	0.50	2.70	0.50	2.80	ns	
$t_{TLH}$ $t_{THL}$	Transition time $Q_n$ or $\bar{Q}_n$		0.45	1.70	0.45	1.70	0.45	1.70	ns
0.45			1.70	0.45	1.70	0.45	1.70	ns	

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC ELECTRICAL CHARACTERISTICS

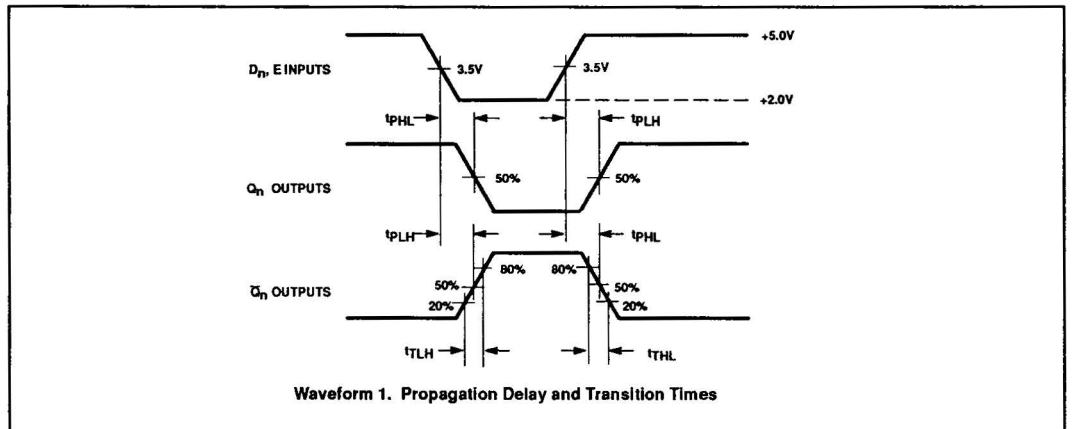
Flat Pack and PLCC  $GND_1 = GND_2 = \text{ground}$ ,  $V_{TTL} = 4.5\text{V to } 5.5\text{V}$ ,  $V_{EE} = -5.2\text{V} \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $D_n$ or $E$ to $Q_n$ or $\bar{Q}_n$	Waveform 1	0.50	2.80	0.50	2.70	0.50	2.80	ns
0.50			2.80	0.50	2.70	0.50	2.80	ns	
$t_{TLH}$ $t_{THL}$	Transition time $Q_n$ or $\bar{Q}_n$		0.45	1.70	0.45	1.70	0.45	1.70	ns
0.45			1.70	0.45	1.70	0.45	1.70	ns	

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC WAVEFORMS



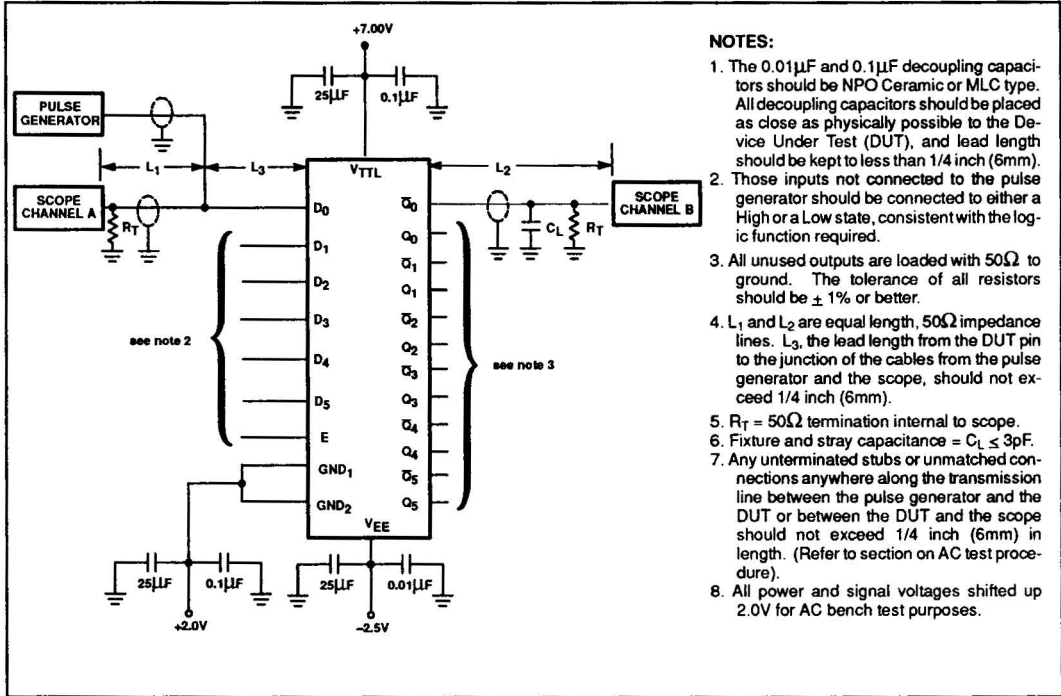
**NOTE:**

All power and signal voltages shifted up 2.0V for AC bench test purposes.

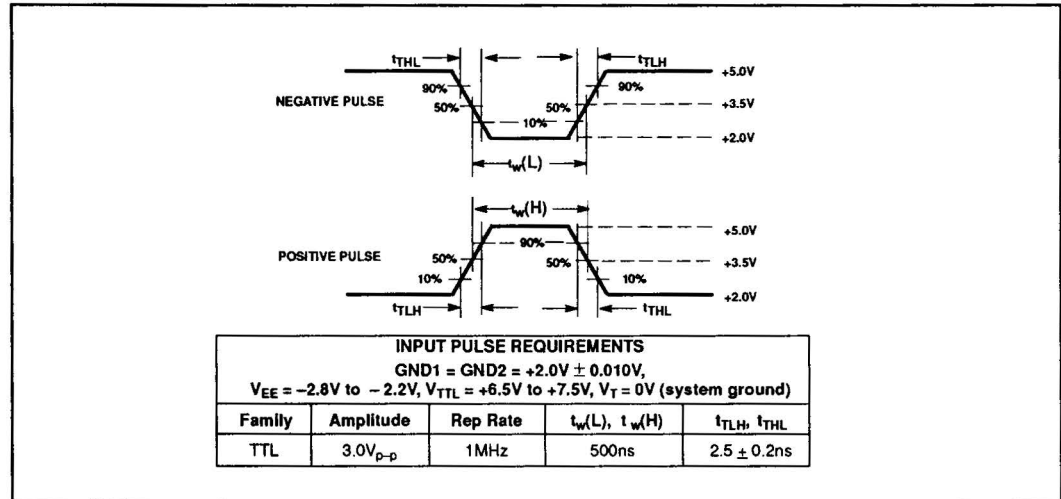
# Translator

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## AC TEST CIRCUIT



## INPUT PULSE DEFINITION



**NOTE:**  
 All power and signal voltages shifted up  $2.0\text{V}$  for AC bench test purposes.