Fractional-N Frequency Synthesizer for DAB Tuner

Description

The U2733B-C is a monolithically integrated fractional-N frequency synthesizer circuit fabricated in TEMIC's advanced UHF5S technology. Designed for applications in DAB receivers, it controls a VCO to synthesize frequencies in the range of 70 to 500 MHz in a 16 kHz raster; four different reference divide factors can be selected. The lock status of the phase detector is indicated at a special output pin, six switching outputs can be addressed. An internal frequency doubler provides an output signal having twice the frequency of the reference oscillator. All functions of this IC are controlled by I^2C bus.

Features

- Microprocessor controlled via I^2C bus
- 4 addresses selectable
- Four reference divide factors selectable:
  1024, 1120, 1152, 1536
- Effectively
- Programmable 15-bit counter 1:2048 to 1:32767 effectively
- Three state phase detector with programmable charge pump
- Superior phase noise performance
- Deactivation of tuning output programmable
- 6 switching outputs (open collector)
- Reference frequency doubler (open collector output)
- Lock status indication (open collector)
- Fully compatible to U2753B-C
- SSO20 package

Block Diagram

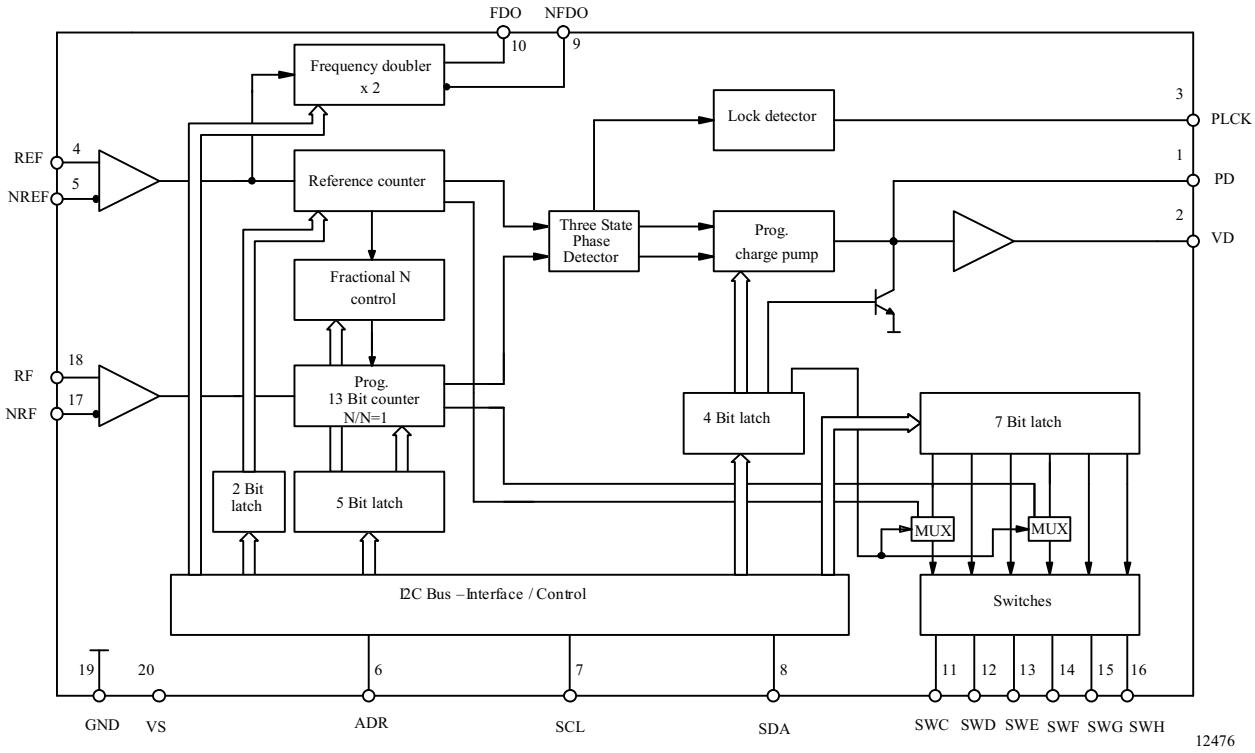


Figure 1. Block diagram

Pin Description

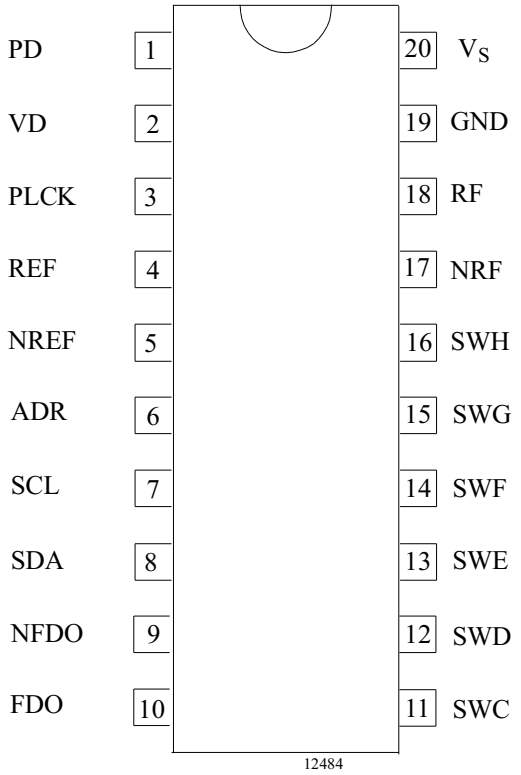


Figure 2. Pinning

Pin	Symbol	Function
1	PD	Three-state charge pump output
2	VD	Active filter output
3	PLCK	Lock indicating output (open collector)
4	REF	Reference input
5	NREF	Reference input (inverted)
6	ADR	Address selection
7	SCL	Clock (I^2C)
8	SDA	Data (I^2C)
9	NFDO	Frequency doubler output (inverted, open collector)
10	FDO	Frequency doubler output (open collector)
11	SWC	Switching output (opencollector)
12	SWD	Switching output (open collector)
13	SWE	Switching output (open collector)
14	SWF	Switching output (open collector)
15	SWG	Switching output (open collector)
16	SWH	Switching output (open collector)
17	NRF	RF input (inverted)
18	RF	RF input
19	GND	Ground
20	V_S	Supply voltage

Functional Description

The U2733B-C is a low power fractional-N frequency synthesizer designed for applications in DAB receivers. Its RF operation range reaches from 70 MHz up to 500 MHz. The device includes input buffers for reference and RF dividers, a reference divider, a programmable RF divider using fractional-N technique, a tri-state phase detector, a programmable charge pump, six switching outputs, a frequency doubler for the reference input signal and a control unit. The control unit has to be accessed by a micro controller via I^2C bus. The programming information is stored in a set of internal registers.

The basic difference of this circuit from the U2753B-C is the use of a special phase noise shaping technique based on the fractional-N principle which concentrates the phase detector's phase noise contribution to the spectrum of the controlled VCO at frequency positions where it doesn't damage the quality of the received DAB signal. In critical locations of the VCO's frequency spectrum the phase detectors phase noise contribution is reduced by roughly 12 dB. A special property of the transmission technique which is used in DAB is that the phase noise weighting function which measures the influence of the LO's phase noise to the phase information of the coded signal in a DAB receiver has zeros, i.e., if phase noise is concentrated in the position of such zeros as discrete lines the DAB signal is not disturbed as long as these lines don't exceed a certain limit.

For DAB mode I this phase noise weighting function is shown in the following figure:

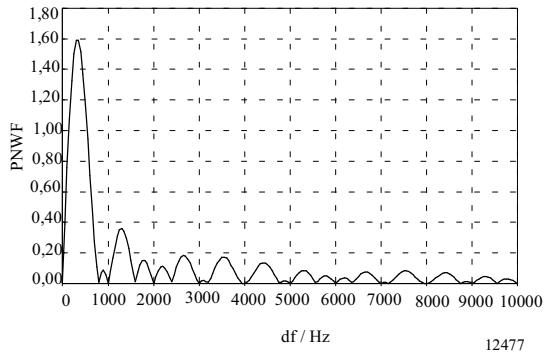


Figure 3.

It is important to realize that this function shows zeros in all distances from the center line which are multiples of the carrier spacing. The technique of concentrating the phase noise in the positions of such zeros is protected by a patent.

In this circuit the phase detector is operated at a frequency which is four times the desired frequency raster spacing (e.g., 16 kHz in case of DAB) and the well known fractional-N technique is used to synthesize the raster. As a result of this technique in the VCO's frequency spectrum spurious occur not only in multiples of the phase detectors input comparison frequency (64 kHz) but also in multiples of the raster frequency (16 kHz). As described above for all DAB modes these spurious are placed in spectral positions where the phase noise weighting function is zero. Therefore no measures are necessary to suppress these lines.

Reference Divider

Four different scaling factors SF_{ref} of the reference divider can be selected by means of the bits 'RD1' and 'RD2' in the I^2C bus instruction code: 256, 280, 288, and 384. Starting from a reference oscillator frequency of 16.384 MHz/ 17.92 MHz/ 18.432 MHz/ 24.576 MHz these scaling factors provide a frequency raster of 64 kHz. By changing the division ratio of the main divider from N to N+1 in an appropriate way (fractional-N technique) this frequency raster is interpolated to deliver a frequency spacing of 16 kHz according to the DAB specification. So effectively the reference divide factors 1024, 1120, 1152 and 1536 can be selected. By setting of the I^2C bus bit 'T' a test signal representing the divided input signal can be monitored at the switching output SWC.

Main Divider

The main divider consists of a fully programmable 13-bit divider which defines a division ratio N. The applied division ratio is either N or N+1 according to the control of a special control unit. On average the scaling factors SF = N+k/ 4 can be selected where k = 0, 1, 2, 3. In this way VCO frequencies

$$f_{VCO} = 4 \times (N+k/4) \times f_{ref}/(4 \times SF_{ref})$$

can be synthesized starting from a reference frequency $f_{ref.}$. If we define $SF_{eff} = 4 \times N+k$ and $SF_{ref,\,eff} = 4 \times SF_{ref}$ we end up with

$$f_{VCO} = SF_{eff} \times f_{ref}/SF_{ref,eff},$$

where SF_{eff} is defined by 15 bits. In the following this circuit is described in terms of SF_{eff} and $SF_{ref,eff}$. SF_{eff} has to be programmed via the I^2C bus interface. An effective scaling factor from 2048 up to 32767 can be selected. By setting of the I^2C bus bit 'T' a test signal representing the divided input signal can be monitored at the switching output SWF.

When the supply voltage is switched on both the reference divider and the programmable divider are kept in RESET state till a complete scaling factor is written onto the chip. Changes in the setting of the programmable divider become active when the corresponding I^2C bus transmission is completed. By an internal synchronization procedure is ensured that such changes don't become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a smooth tuning of the output frequency without disturbing the controlled VCO's frequency spectrum.

Phase Comparator and Charge Pump

The tri-state phase detector causes the charge pump to source or to sink current at the output pin PD depending on the phase relation of its input signals which are provided by the reference and the main divider respectively. Four different values of this current can be selected by means of the I^2C bus bits 'I50' and 'I100'. By use of this option for example changes of the loop characteristics due to the variation of the VCO gain as a function of the tuning voltage can be reduced. The charge pump current can be switched off using the I^2C bus bit 'TRI'. A change in the setting of the charge pump current becomes active when the corresponding I^2C bus transmission is completed. As described for the setting of the scaling factor of the programmable divider an internal synchronization procedure ensures that such changes don't become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a change in the charge pump current without disturbing the controlled VCO's frequency spectrum.

A high gain amplifier (output pin: VD) which is implemented in order to construct a loop filter as shown in the application circuit can be switched off by means of the I²C bus bit 'OS'.

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If phase lock is detected the open collector output pin PLCK is set 'H' (logical value!). It should be noted that the output current of this pin must be limited by external circuitry as it is not limited internally. If the I²C bus bit 'TRI' is set 'H' the lock detector function is deactivated and the logical value of the PLCK output is undefined.

Switching Outputs

Six switching outputs controlled by the I²C bus bits 'SWC', 'SWD', 'SWE', 'SWF', 'SWG', 'SWH' can be used for any switching task on the front end board. The currents of these outputs are not limited internally. They have to be limited by external circuitry.

Frequency Doubler

An internal frequency doubler provides a signal at twice the frequency of the reference signal appearing at the input pins REF and NREF. If the I²C bus bit 'OFD' = 'H' the current of its open collector outputs FDO and NFDO is doubled. By means of the I²C bus bit 'OFD' the frequency doubler function can be switched off.

As shown on page 15 (Integration in TEMIC DAB Receiver Concept) the output signal of the frequency doubler can be used in order to construct the LO signal of the IF circuit (U2759B).

I²C Bus Interface

Via its I²C bus interface various functions can be controlled by a microprocessor. These functions are overviewed in the following sections 'I²C bus instruction codes' and 'I²C bus functions'. By means of the ADR pin four different I²C bus addresses can be selected as described in the section 'Electrical characteristics'.

I²C Bus Instruction Codes

Description	MSB							LSB
Address byte	1	1	0	0	0	AS1	AS2	0
Divider byte 1	0	RD1	RD2	X	X	n_{14}	n_{13}	n_{12}
Divider byte 2	X	X	n_{11}	n_{10}	n_9	n_8	n_7	n_6
Divider byte 3	X	X	n_5	n_4	n_3	n_2	n_1	n_0
Control byte 1	1	X	0	OS	T	TRI	I100	I50
Control byte 2	OFD	2IFD	SWC	SWD	SWE	SWF	SWG	SWH
Control byte 3	X	0	0	0	0	0	0	0

I²C Bus Functions

AS1, AS2 define the I²C bus address

RD1, RD2 define the effective scaling factor of the reference divider:

RD1	RD2	Effective Scaling Factor
0	0	1120
1	0	1152
0	1	1024
1	1	1536

n_i effective scaling factor (SF_{eff}) of the main divider $SF_{eff} = SUM(n_i\ 2^i)$

OS OS = 'H' switches off tuning output

T for T = 'H' reference signals describing the output frequencies of reference reference divider and programmable divider are monitored at SWF (prog. div.) and SWC (ref. div.)

TRI TRI = 'H' switches off charge pump

I50, I100 define the charge pump current:

I50	I100	Charge Pumup Current (nominal)/A
'L'	'L'	50
'H'	'L'	102
'L'	'H'	151
'H'	'H'	203

OFD OFD = 'H' switches off frequency doubler

2IFD 2IFD = 'H' doubles the frequency doubler output current

SWa SWa = 'H' switches on output current

I²C Bus Data Transfer

Format

START – ADR – ACK – <instruction set> – STOP

The <instruction set> consists of a sequence of divider bytes and control bytes each followed by ACK. Divider byte i must be followed by divider byte i+1 (control byte 1 if i = 3) or the instruction set must be finished. Control bytes have to be handled accordingly.

Examples

START – ADR – ACK – DB1 – ACK – DB2 – ACK – DB3 – ACK – CB1 – ACK – CB2 –ACK – CB3 – ACK – STOP

START – ADR – ACK – CB1 – ACK – CB2 – ACK – STOP

However

START – ADR – ACK – DB1 – ACK – CB1 –ACK – STOP is not allowed.

Description

START start condition

STOP stop condition

ACK acknoledge

ADR address byte

DBi divider byte i (i = 1, 2, 3)

CBi control byte i (i = 1, 2, 3)

I²C Bus Timing

The values of the drawn periods are specified in the section 'Electrical Characteristics'. More detailed informations can be taken from 'Application Note 1.0 (I²C Bus Description)'. Please note: due to the I²C bus specification the MSB of a byte is transmitted first, the LSB last.

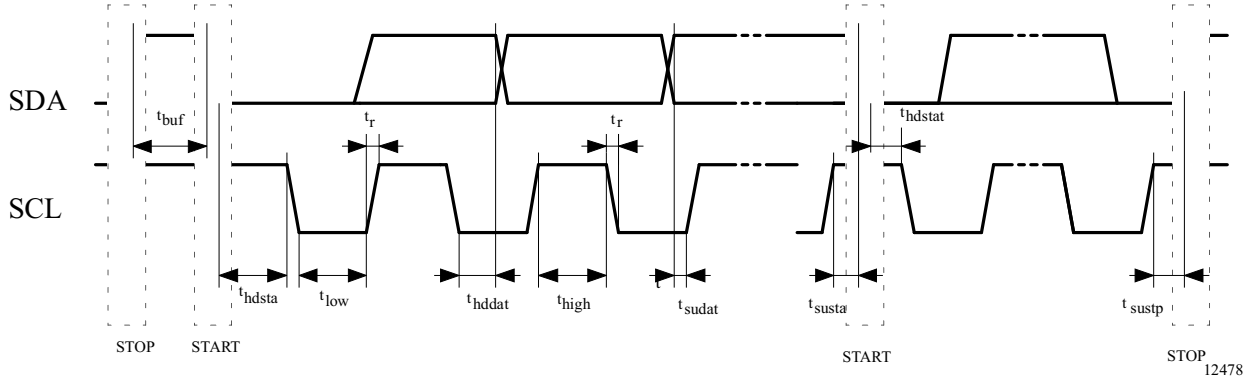


Figure 4.

Typical Pulse Diagram

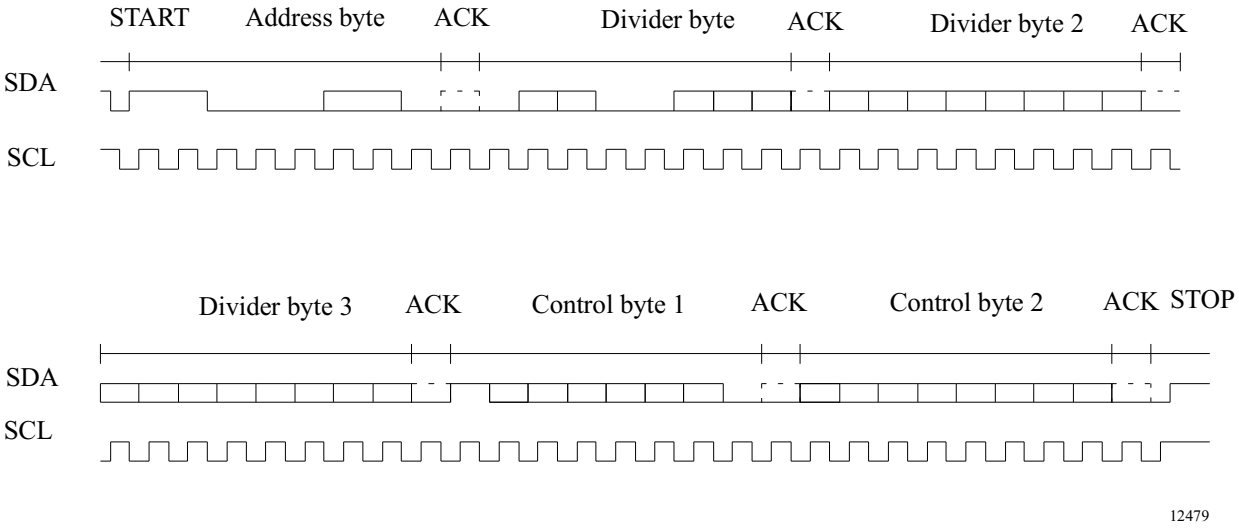


Figure 5.

Absolute Maximum Ratings

Parameter	Pin	Conditions	Value	Unit
Supply voltage	VS		–0.3 to 5.5	V
RF input voltage (AC)	RF, NRF		1	V_{pp}
Reference input voltage (AC)	REF, NREF		1	V_{pp}
I^2C bus input/ output voltage	SCL, SDA		–0.3 to V_S	V
SDA output current	SDA		5	mA
Address select voltage	ADR		–0.3 to V_S	V
Switch output current	SW_a	Open collector	4	mA
Switch output voltage	SW_a	Open collector	–0.3 to 5.5	V
PLCK output current	PLCK	Open collector	0.5	mA
PLCK output voltage	PLCK	Open collector	–0.3 to 5.5	V
Frequency doubler output	FDO, NFDO	Open collector	V_S –1 to 5.5	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}		–40 to 125	°C

Operating Range

Parameter	Pin	Conditions	Value	Unit
Supply voltage	V_s		4.5 to 5.5	V
Ambient temperature range	T_{amb}		–30 to+85	°C

Thermal Resistance

Parameter	Pin	Conditions	Value	Unit
Junction ambient	R_{thJA}	SSO20	140	K/W

Electrical Characteristics

Test conditions: V_S = 5 V, T_{amb} = 27°C, unless otherwise specified

Characteristics	Pin	Symbol	Conditions	Min.	Typ.	Max	Unit
Supply current	V_s	I_s	SW_a='L',TRI='L', PLCK='L',OS='L', I50='H', I100='H', OFD='L',2IFD='L'	13.2	16.5	19.8	mA
		I_{so}	SW_a='L',TRI='L', PLCK='L',OS='L', I50='H', I100='H', OFD='H',2IFD='L'		14.6		mA
Effective scaling factor of programmable divider		SF_{eff}		2048		32767	
Effective scaling factor of reference divider		$SF_{ref,eff}$	RD1='L',RD2='L' RD1='H',RD2='L' RD1='L',RD2='H' RD1='H',RD2='H'		1120 1152 1024 1536		
Tuning step		f_{rast}	17.920 MHz/ 18.432 MHz/ 16.384 MHz/ 24.576 MHz ref. frequency		16		kHz
RF input	RF, NRF						
Input frequency range		f_{rf}	V_S = 4.5 V, T_{amb} = 20°C	70		500	MHz
Input sensitivity		V_{rfs}			10	20	mV_{rms}
Max. input signal		V_{rfmax}				300	mV_{rms}
Input impedance		Z_{rf}	Differential		200		
VSWR		$VSWR_{rf}$			2		
REF input	REF, NREF						
Input frequency range		f_{ref}	V_S = 4.5 V, T_{amb} = 20°C	5	17.92 18.432	30	MHz
Input sensitivity		V_{refs}			10		mV_{rms}
Max. input signal		V_{refmax}				300	mV_{rms}
Input impedance		Z_{ref}	Single ended		2.7 ‖2.5		k pF
Phase detector	PD						
Charge pump current		$\pm I_{PD4}$	I100='H', I50='H'	± 160	± 203	± 240	A
		$\pm I_{PD3}$	I100='H', I50='L'	± 120	± 151	± 180	A
		$\pm I_{PD2}$	I100='L', I50='H'	± 80	± 102	± 120	A
		$\pm I_{PD1}$	I100='L', I50='L'	± 40	± 50	± 60	A
		$\pm I_{PD,tri}$	TRI = 'H'			± 100	nA
Effective phase noise *)		L_{PD}	I_{PD}=203A		–163		dBc/Hz
Lock indication	PLCK						

Characteristics	Pin	Symbol	Conditions	Min.	Typ.	Max	Unit
Leakage current		$I_{PLCK,L}$	V_{PLCK} = 5.5 V			10	A
Saturation voltage		$V_{PLCK,sat}$	I_{PLCK} = 0.5 mA			0.5	V
Frequency doubler	FDO, NFDO						
Output current		I_{FDOL}, I_{NFDOL}	$V_{FDO} = V_S$, $V_{NFDO} = V_S$, 2IFD = 'L'	0.4	0.5	0.6	mA_{pp}
		I_{FDOH}, I_{NFDOH}	$V_{FDO} = V_S$, $V_{NFDO} = V_S$, 2IFD = 'H'	0.8	1.0	1.2	mA_{pp}
Minimum output voltage		V_{FDO}, V_{NFDO}	V_S = 5 V	4			V
Switches	SWa						
Leakage current		$I_{SW,L}$	V_{SWa} = 5.5 V			10	A
Saturation voltage		$V_{SW,sat}$	I_{SWa} = 4 mA			0.5	V
Address selection	ADR						
AS1=0, AS2=0				0		0.1 V_S	
AS1=0, AS2=1					open		
AS1=1, AS2=0				0.4 V_S		0.6 V_S	
AS1=1, AS2=1				0.9 V_S		V_S	
I^2C bus	SCL, SDA						
Input voltage SCL/SDA		V_H	'High'	3		5.5	V
		V_L	'Low'			1.5	V
Output voltage SDA (open collector)			I_{SDA} = 2mA SDA = 'L'			0.4	V
SCL clock frequency		f_{SCL}		0.1		100	kHz
Rise time (SCL, SDA)		t_r				1	s
Fall time (SCL; SDA)		t_f				300	ns
Time before new transmission can start		t_{buf}		4.7			s
SCL 'H' period		t_{high}		4			s
SCL 'L' period		t_{low}		4.7			s
Hold time START		t_{hdsta}		4			s
Set up time START		t_{susta}		4.7			s
Set up time STOP		t_{sustp}		4.7			s
Hold time DATA		t_{hddat}		0			s
Set up time DATA		t_{sudat}		250			ns

*) The phase detectors phase noise contribution to the VCO's frequency spectrum is refered to the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Application Circuit

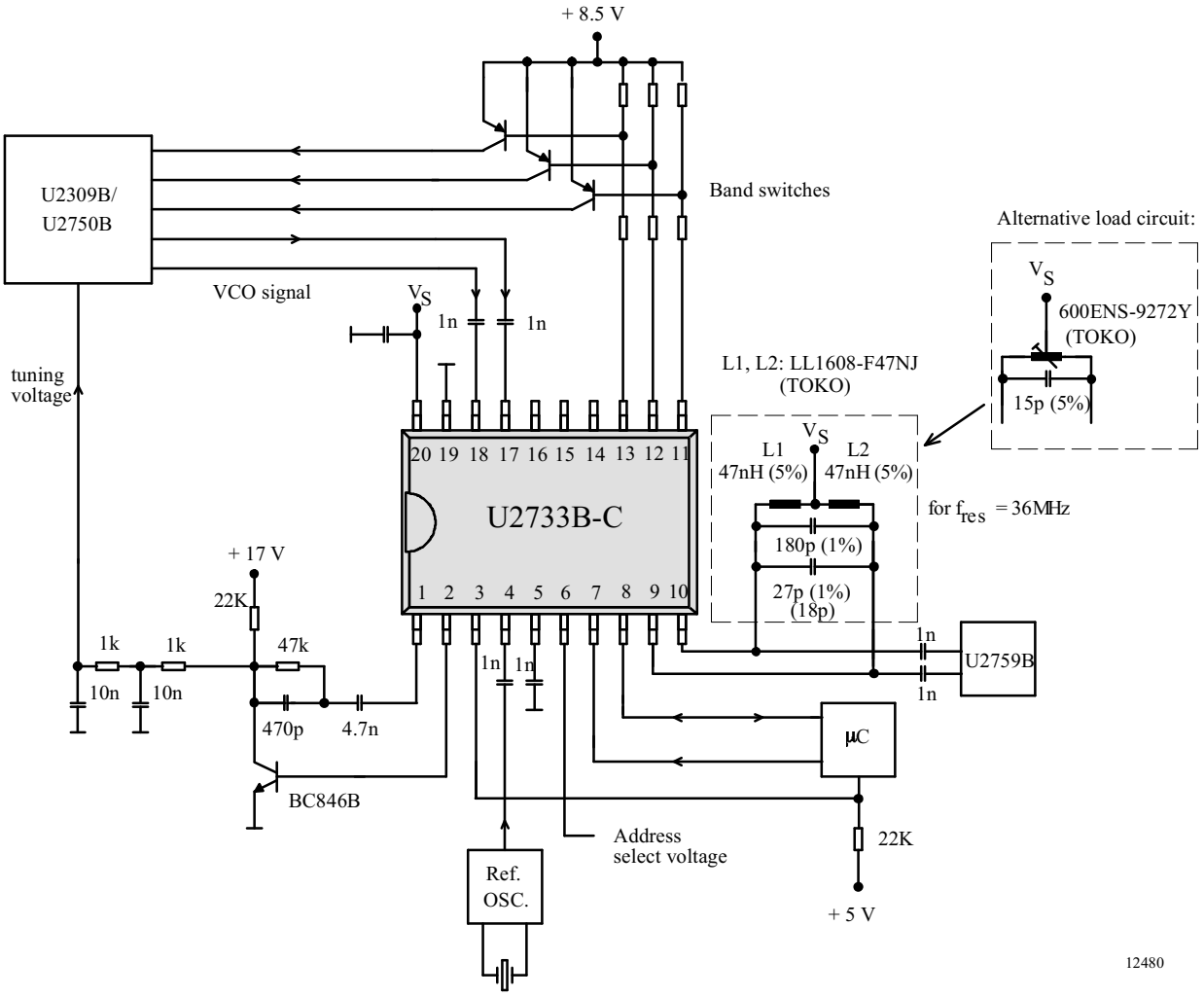


Figure 6. Application circuit

Phase Noise Performance

(Example: SF_{eff} = 16899, $SF_{ref,eff}$ = 1120, f_{ref} = 17.92 MHz, I_{PD} = 200 A, reference oscillator: MARCONI INSTRUMENTS signal generator 2042, spectrum analysis: HP70000, above shown application circuit, band A oscillator of U2309B)

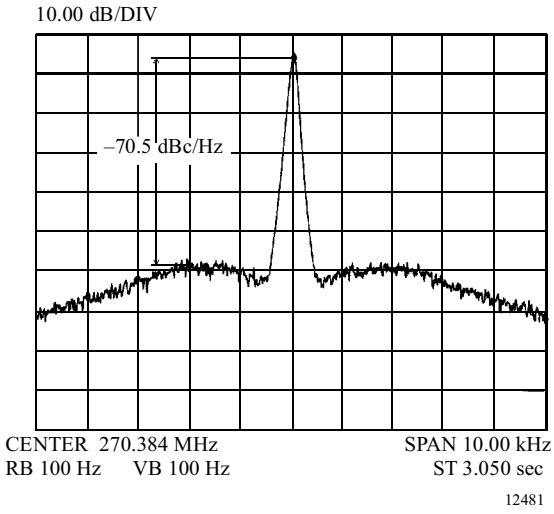


Figure 7.

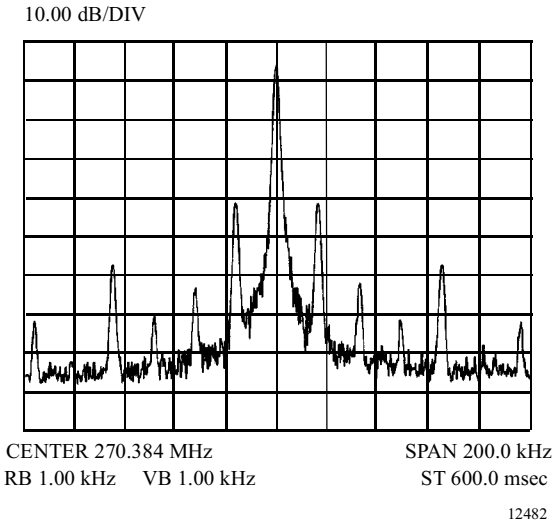


Figure 8.

Integration in TEMIC DAB Receiver Concept

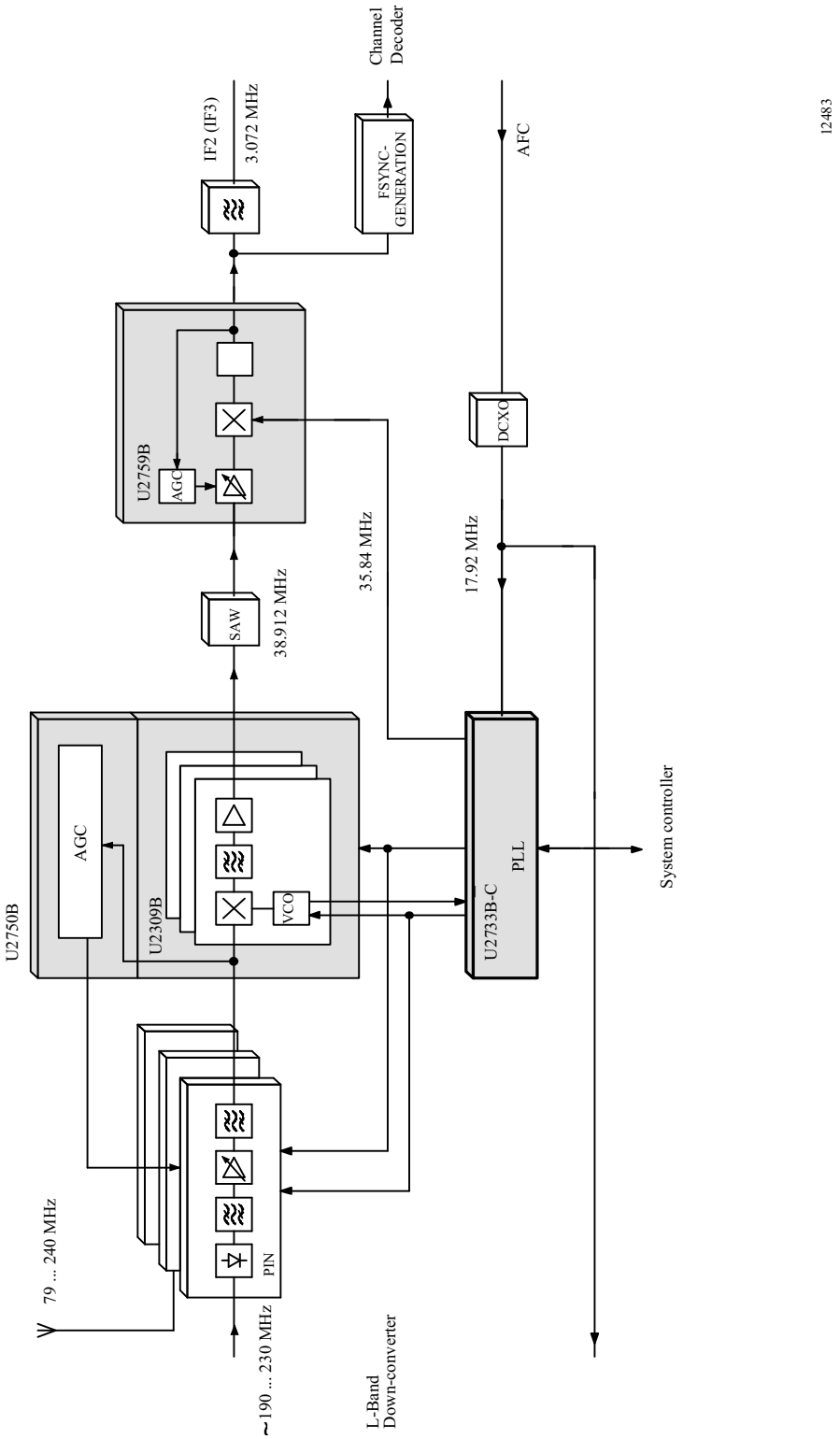
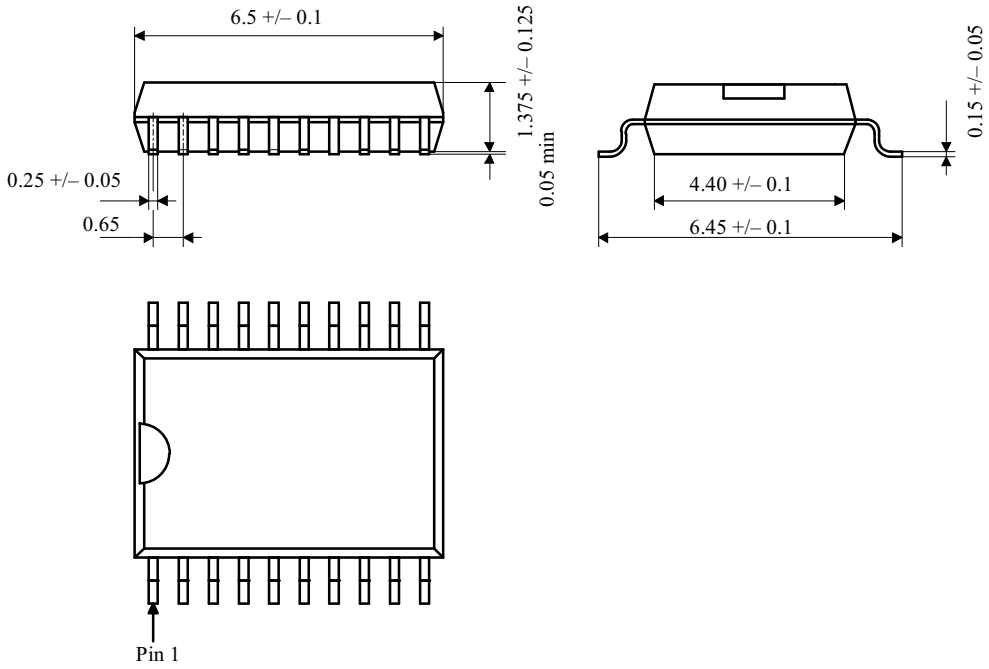


Figure 9. DAB Receiver Frontend

Package Dimensions

SSO20 all dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.
Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423